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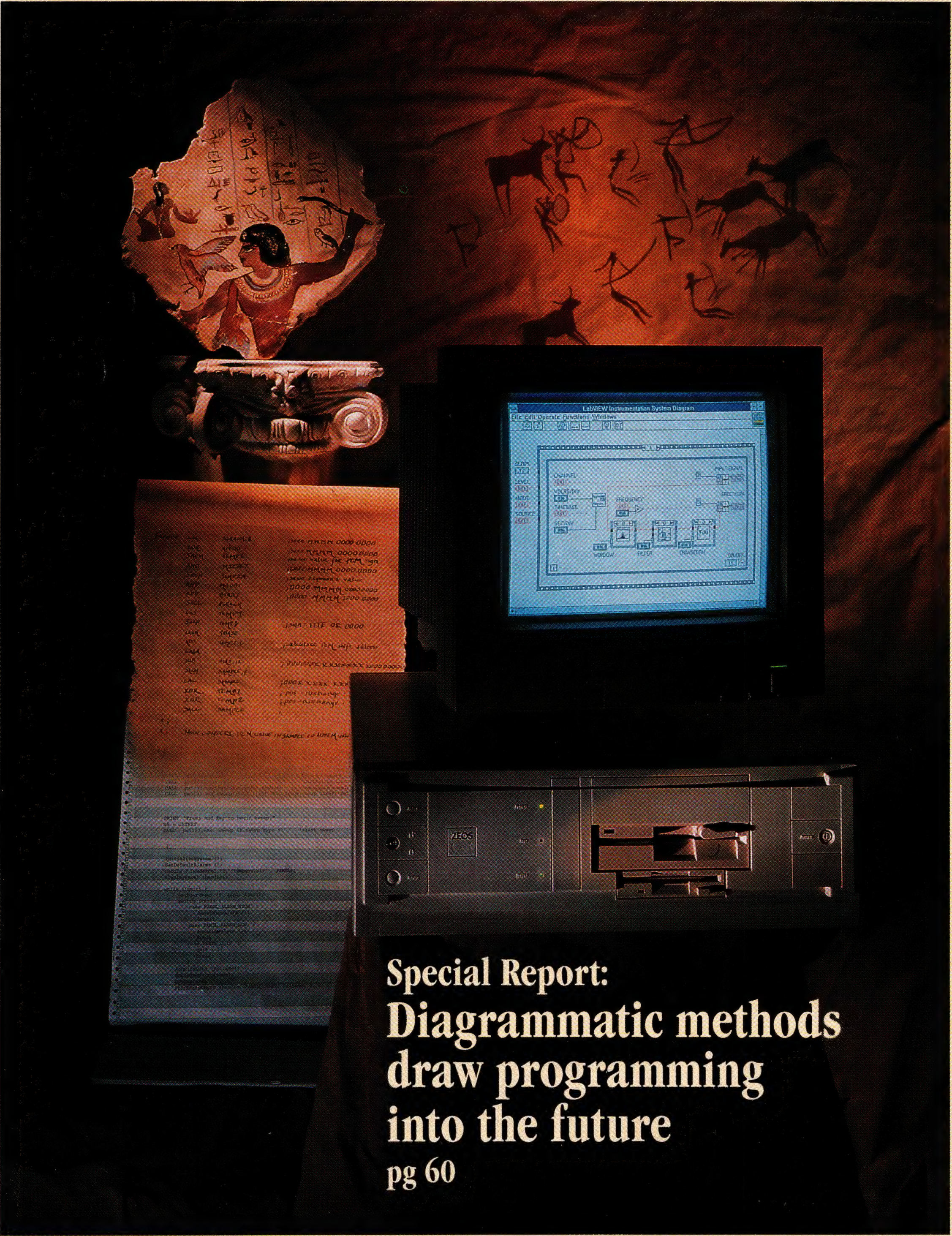
THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

11 MAR 1994

January 6, 1994


LabVIEW Instrumentation System Diagram
File Edit Operate Functions Windows
ZEOS

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Diagrammatic methods draw programming into the future

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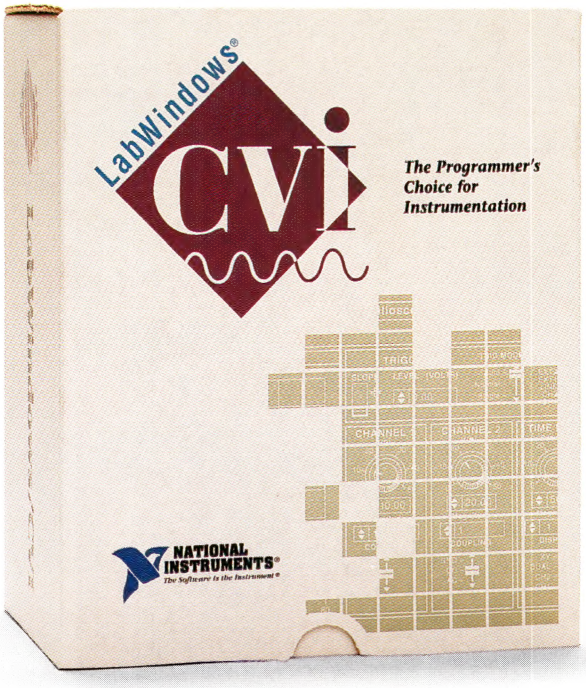
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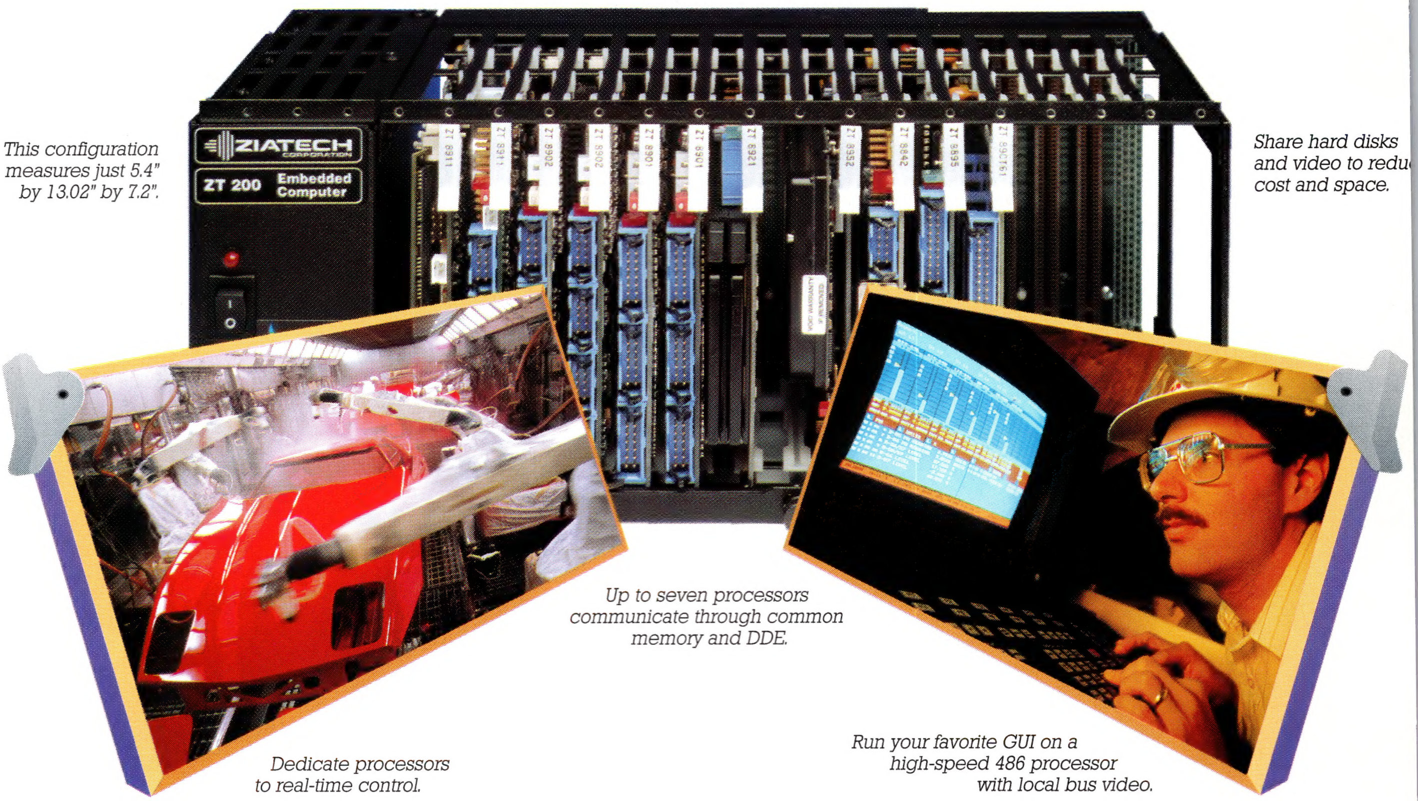

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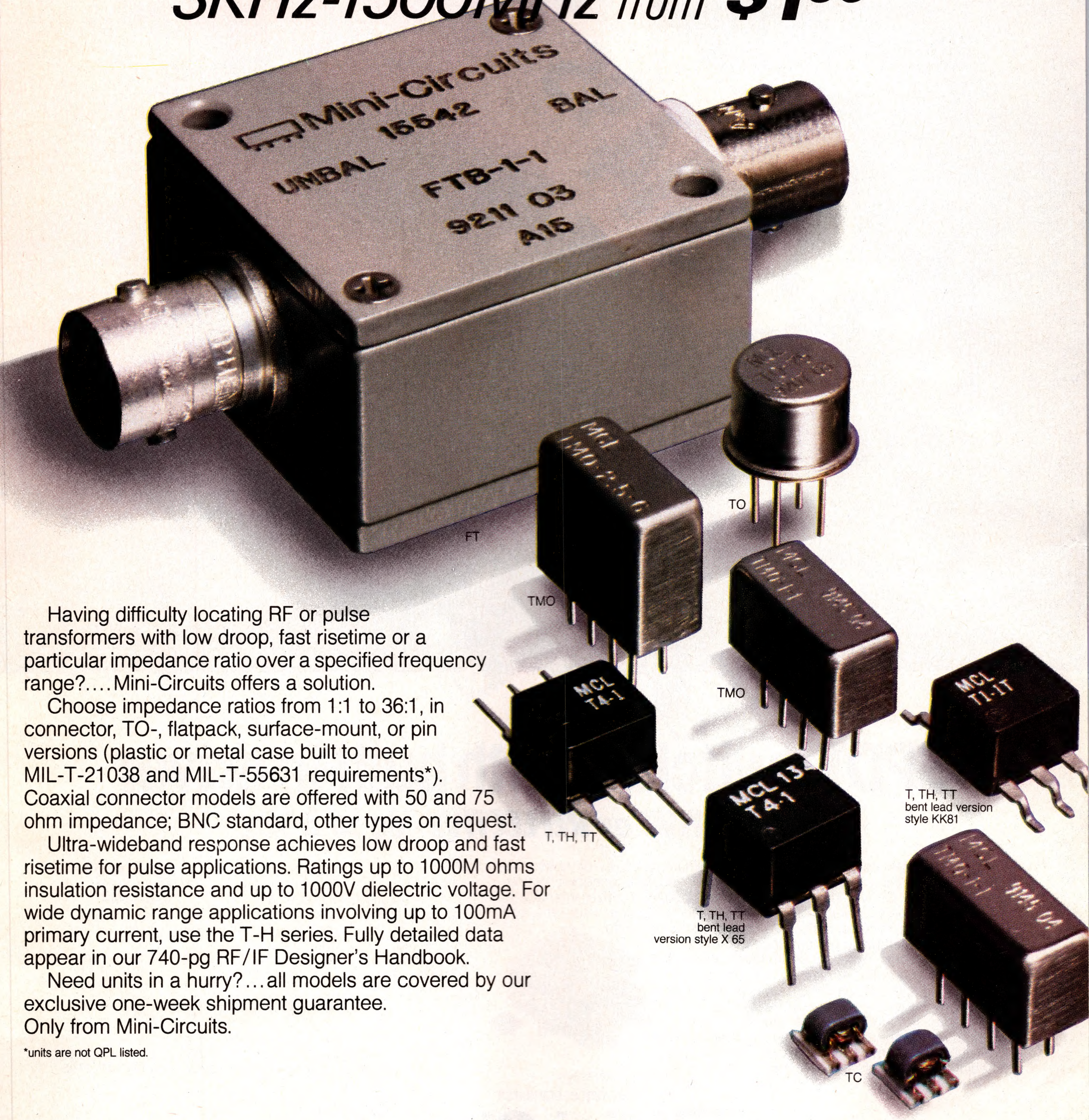

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RF Input (max dBm)	——	20	——	22	22	26
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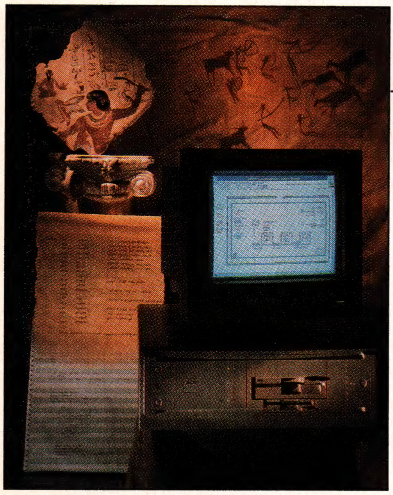

On the cover: Programming has come a long way, from typing endless strings of ASCII characters to actually drawing your program. See our Special Report, beginning on .... **PG 60.** (Photo courtesy National Instruments; art director, Sandra Stephens; photographer, James Minor; photography coordinator, Lara Farwell)

SPECIAL REPORT

Diagrammatic programming 60

A host of diagrammatic-programming and debugging tools allows you to picture what your program *is* rather than making you describe in words what it does.—*Charles H Small, Senior Technical Editor*

DESIGN FEATURES

Techniques illuminate backlit LCDs with high efficiency 89

Getting a backlight LCD lamp to turn on is just the first step in the design process. Achieving and maintaining high efficiency requires attention to both circuit-design *and* physical-layout details.
—*Jim Williams, Linear Technology Corp*

Phase compensation counteracts op-amp input capacitance 97

Although op amps are mature devices, many designers often ignore the effects of input capacitance on frequency stability. A bode plot analysis lets you add compensation capacitors to counteract poles and zeros caused by an op amp's input capacitance.
—*Jerald Graeme, Burr-Brown Corp*

DESIGN IDEAS

Modulator's design cuts FPGA's gate count 79
Line driver economically synthesizes impedance 79
Converter has high efficiency at low loads 80
Classic detector enables low-cost receiver 80
Spice subcircuit simulates any second-order filter 84
Simple circuit detects current pulses 84
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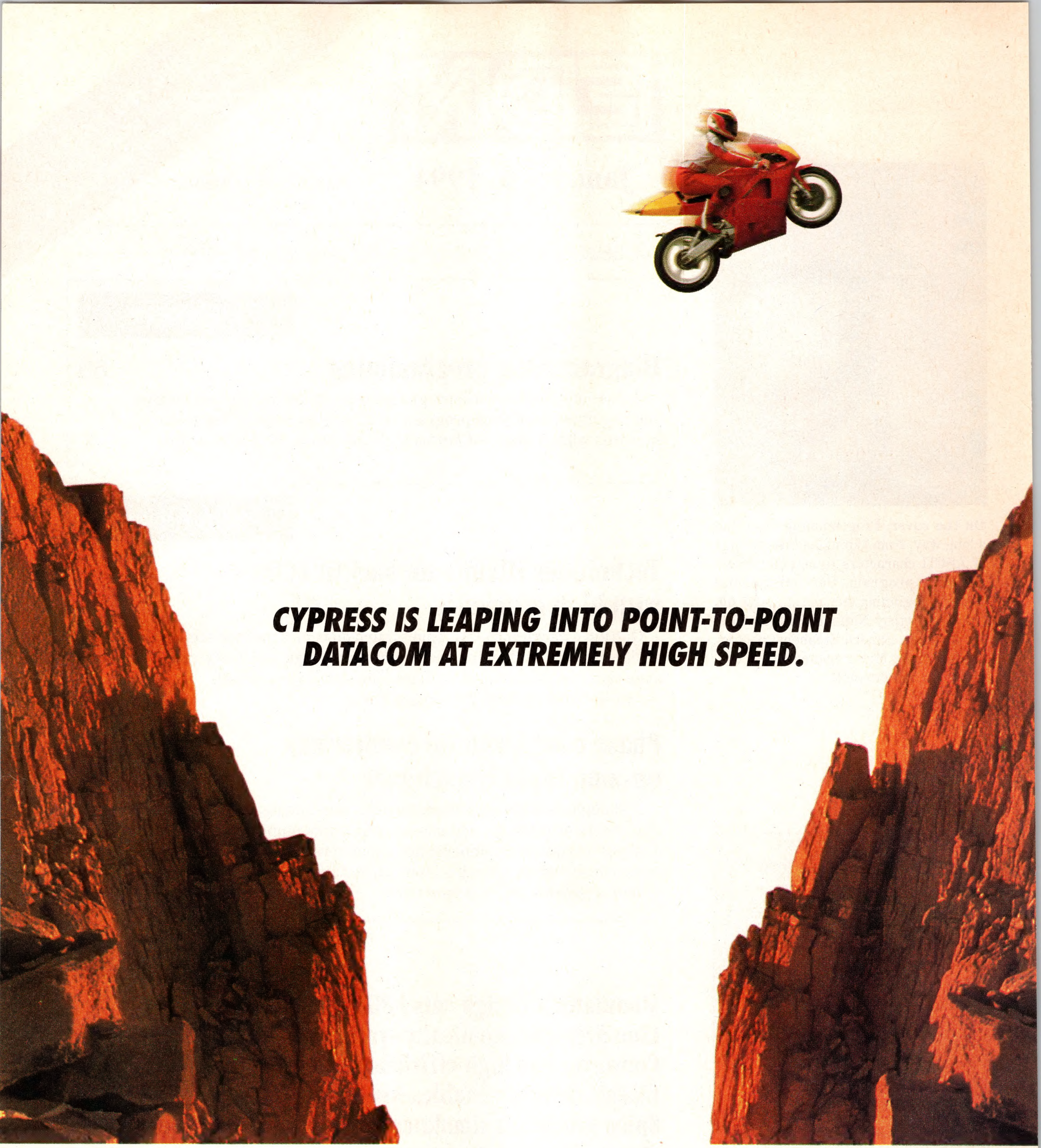
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January 6, 1994

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TECHNOLOGY UPDATES

Emerging 100-Mbit Ethernet standards ease system bottlenecks 35

The networking industry is developing faster versions of Ethernet to meet increasing demands for LAN capacity. As a result, two standards are now emerging—each reflecting a different cost or capability tradeoff.—*Richard A Quinnell, Technical Editor*

Handheld-receiver front ends integrate assorted components 49

Front-end products for handheld wireless receivers include amplifiers, spdt switches, antennas, attenuators, and filters. Unfortunately, most of these devices come as separate components, which the system manufacturer must wire together.
—*John Gallant, Technical Editor*

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—*Charles H Small, Senior Technical Editor*

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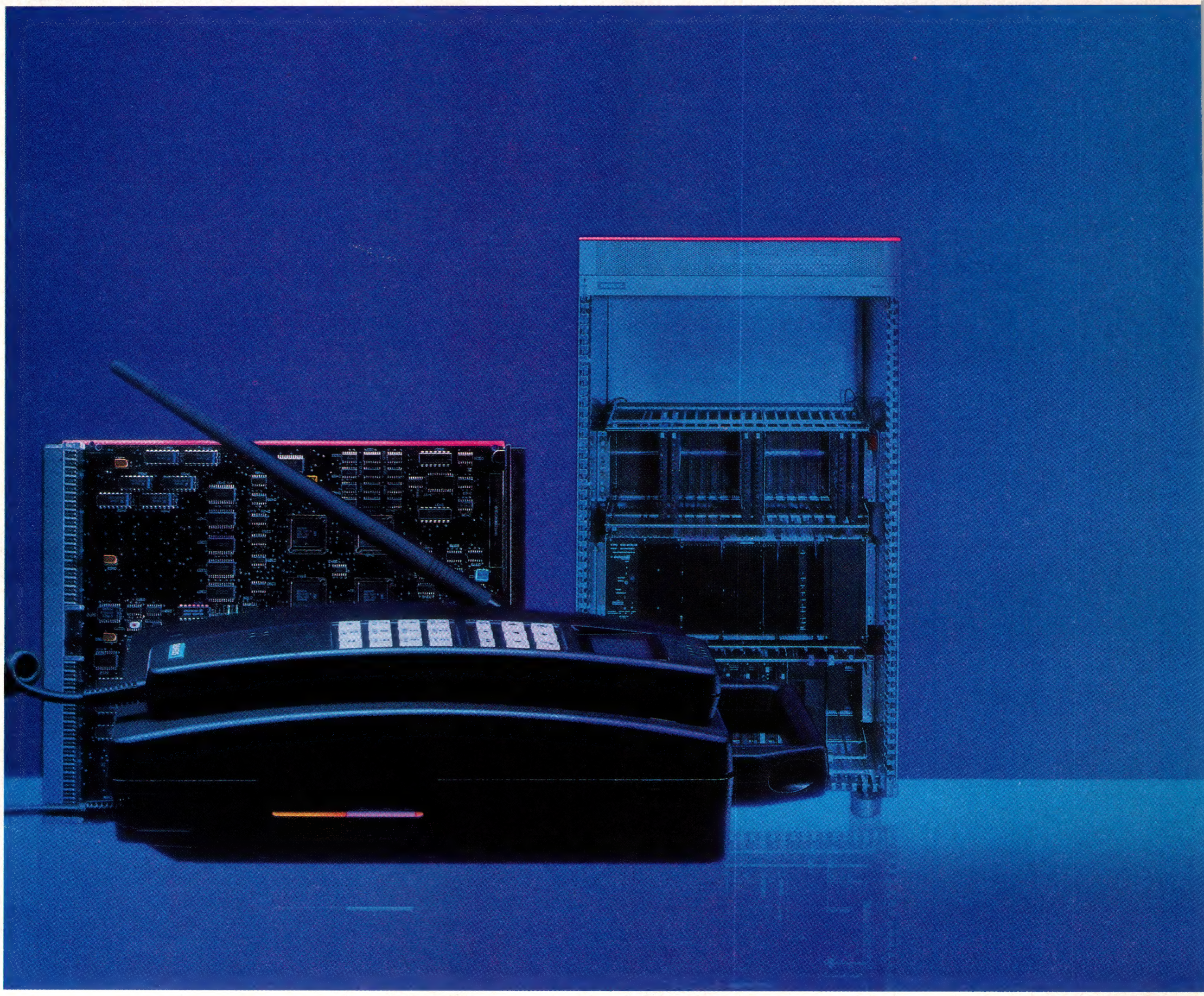

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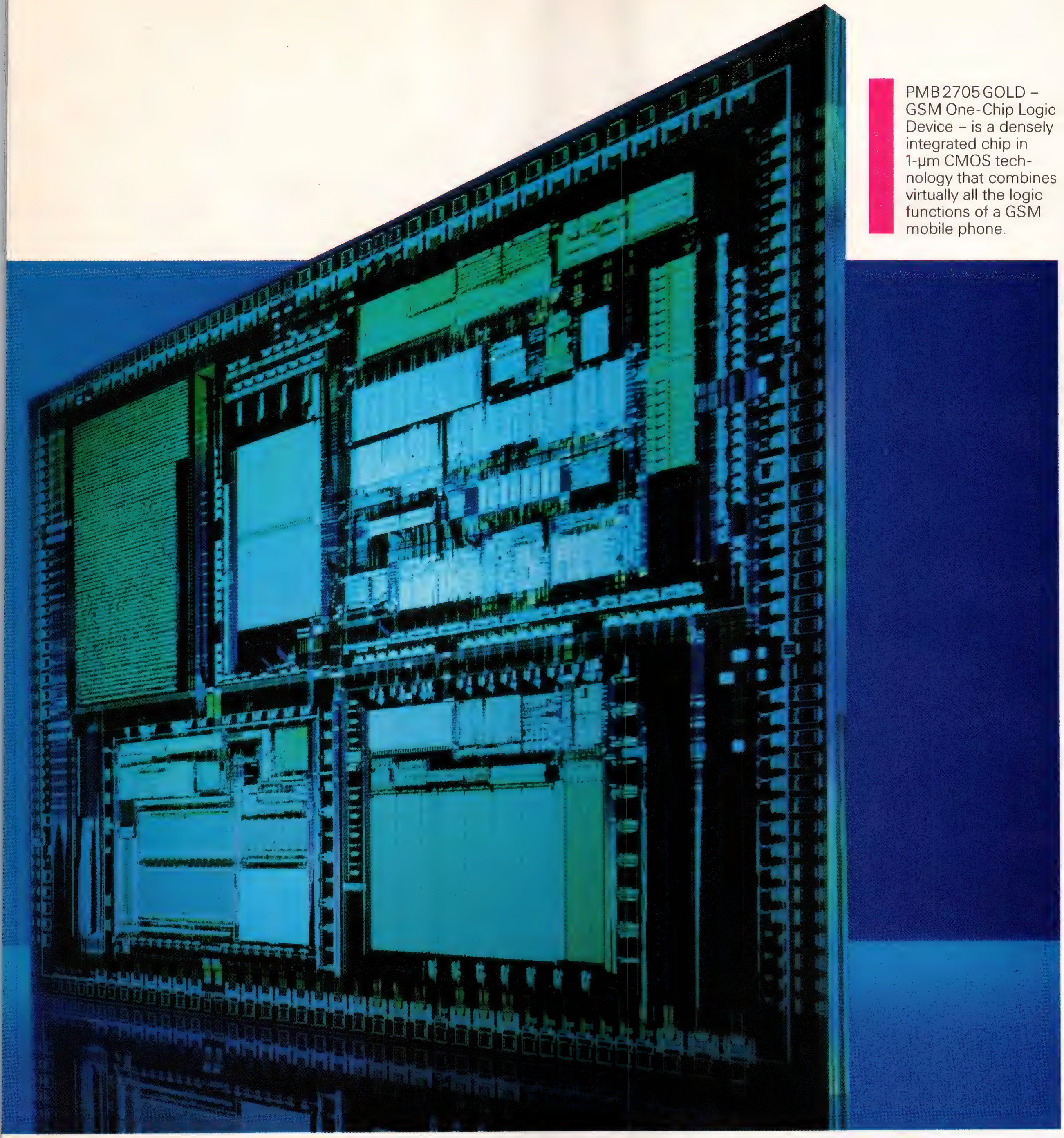

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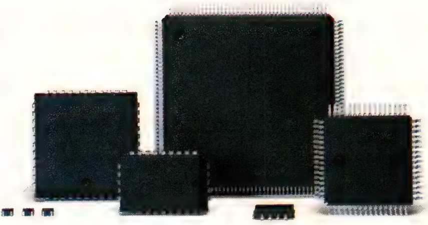

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How to sandwich more on a motherboard.

With real estate at a premium, designers are looking for new ingredients in the recipe for high-density packaging.

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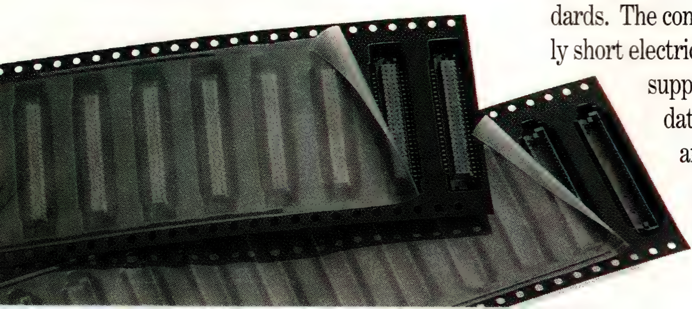

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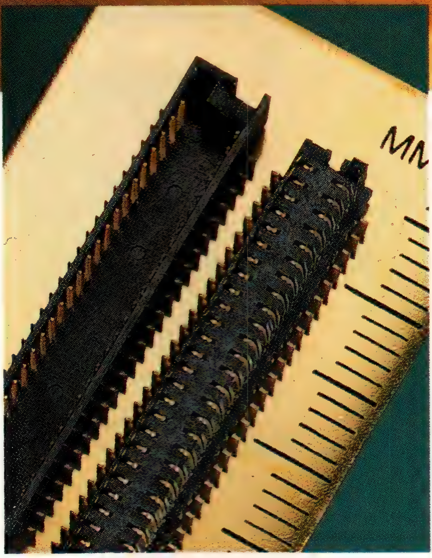

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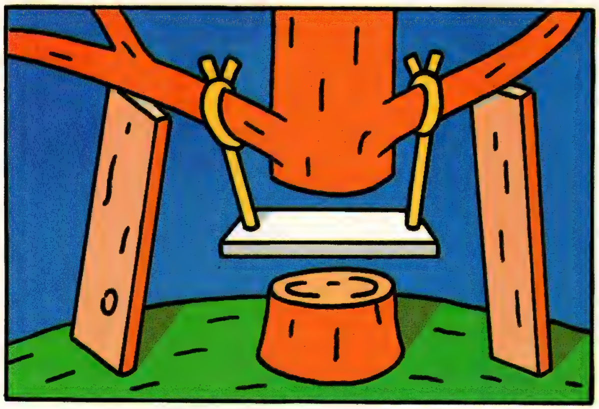

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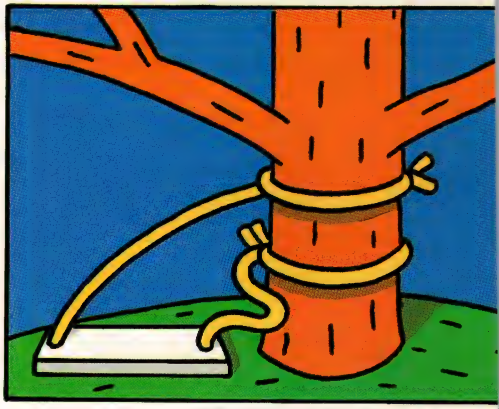

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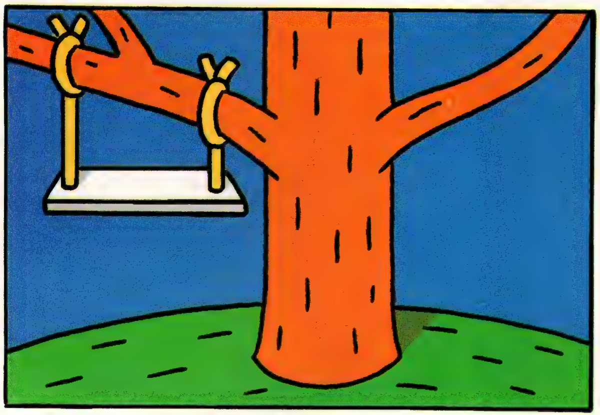

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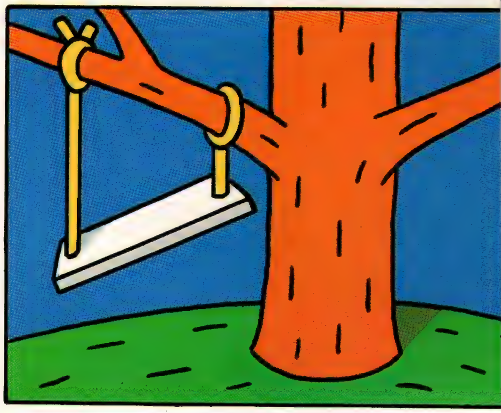

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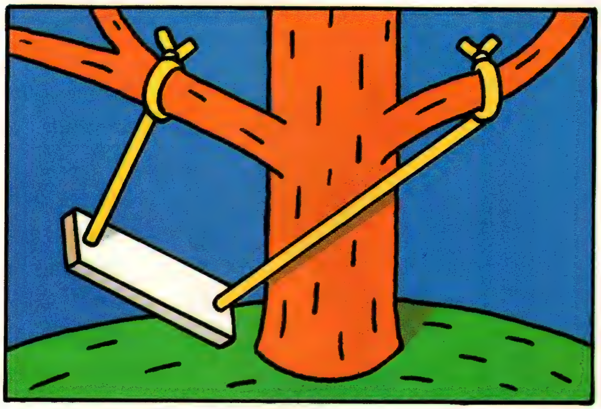

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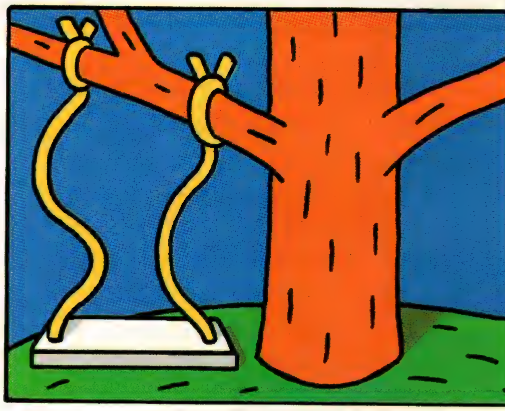
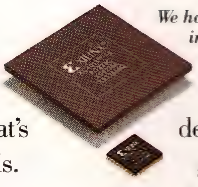


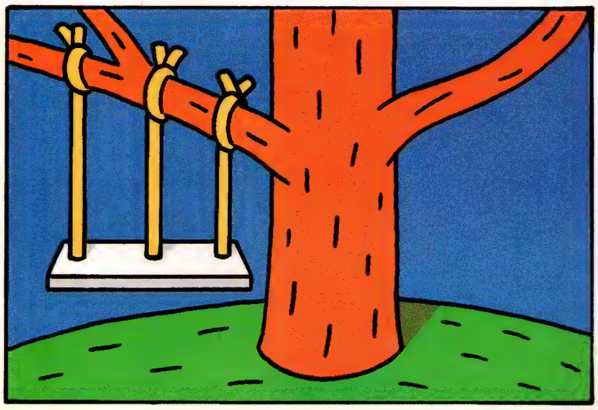
What Documentation Described



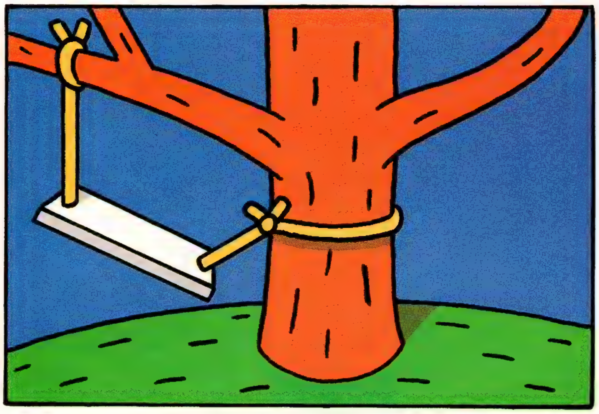
We have as many options as you need (more than 350, in fact), from our new 13,000 gate XC4013 FPGA, to our space-saving TQFP.

Look familiar?

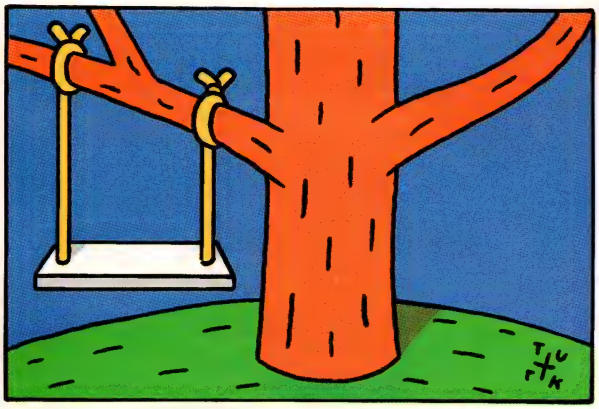
We're willing to bet a sizable chunk of next week's pay that a cartoon like this hangs in just about every engineering department in this country.



What Management Agreed On



How Marketing Changed It



What The Customer Wanted

Why?

Because that's just the way it is.

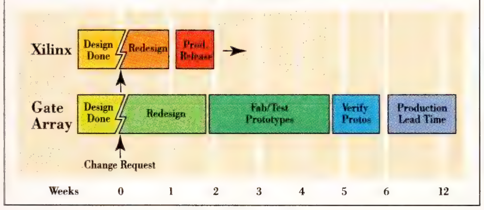
So given the amount of miscalculation, miscommunication, and misdirection you have to deal with, why not choose a logic device that won't let you go wrong?

Nothing does that better than an FPGA from Xilinx.

First of all, since we make more than 350 different speed grades, densities, and packages, you can get off to a flying start with just the right part.

Then, with our powerful XACT™ Development System, you can work with your design down to the gate level if necessary, to get it right, right off the bat.

Race to Market



With FPGAs from Xilinx, you can get to market faster even if you make a ton of changes — all in less time than a single gate array change cycle.

But even if you can't get your first design to fly (or the guys in marketing change their minds), there's no problem. You and your colleagues can go back and forth as often as you like.

Because you can change a Xilinx FPGA as often as you like, with no hard feelings. And no added expense.

In fact, you can even make changes right in the system, because our devices are reprogrammable.

And since Xilinx FPGAs are never actually changed –just programmed–they won't hang you with too much inventory–or worse –not enough.

What will all this flexibility cost you?

A better question might be, What will it cost you not to have it?

After all, when you consider the financial consequences of getting into the market later rather than sooner, Xilinx FPGAs may just be the best investment you can make.

They can save you time, they can save you money, they can save you, period.

And all because they're made for a world where imperfection isn't just a sometime occurrence, but a daily reality.

To learn more about how we can help you cope with the ups and downs of engineering in the '90s, call our 24-hour literature hotline at 800-231-3386, or talk to your Xilinx representative.

We'll be perfectly happy to give you a push in the right direction.

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Logic Company.℠

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CIRCLE NO. 47

Quicker. Easier.
To save you time.

To get solutions quickly, carry the best portable tool for engineering computation. The HP 48G graphic calculator. Focused problem-solving environments in the HP 48G lead you to answers fast.

Press ↰ and EQUATION. Create equations that look the same way you'd write them. Press ↱ and SOLVE. Then just choose the kind of problem you want to solve. Like differential equations, a system of linear equations, or others. It's your choice.

You'll quickly
learn to operate it!

Pull-down menus guide you through problem-solving smoothly and quickly. Push a button, select an entry from the pull-down menu, and fill in the blanks. Entering data is that easy.

The tool you would have designed for yourself!

Technically sophisticated. It contains over 300 built-in equations grouped into 15 technical subjects. Electricity, forces and energy, stress analysis, and other technical categories.

And, it lets you work with many different object types for solving problems. Real numbers with units, polar forms of complex numbers, symbolic constants, variables in formulas, matrices, and lots more. It's an engineer's dream tool!

Special money-saving offer on Sparcom's CalcWare PC/Mac Link software and connectivity cable.

The HP 48G (and its RAM card expandable cousin, the HP 48GX) can be linked to your desktop PC or Mac. Sparcom is offering a special $49.95 price ($10.00 off) on its HP 48 CalcWare PC/Mac Link. This connectivity software and cable are being offered at a special price from October 1, 1993 until June 30, 1994.

To get more information on the HP 48 along with this and other special Sparcom offers, call 800-443-1254, Dept. 421.

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EDITED BY FRAN GRANVILLE

Alliances create networking partnerships

National Semiconductor is moving to expand its presence in the networking market with a pair of partnerships. In separate agreements, National has teamed with Novell and with NEC to develop Ethernet silicon, software, and system products.

The agreement between Novell and National Semiconductor calls for integrating their two product lines, beginning with a joint offering of PCMCIA Ethernet and FDDI cards. The companies will also be jointly developing hardware and software for video on Ethernet and asynchronous-transfer-mode (ATM) networks.

The agreement with NEC moves to expand the Ethernet market in Japan in two ways. The first is by having NEC market National Semiconductor's Ethernet board products under the NEC logo. The second is by jointly developing a low-power version of National's Sonic-T Ethernet-controller IC. The companies seek to enable development of network-ready "green" PCs in Japan.—by Richard A Quinnell

National Semiconductor, Santa Clara, CA, (800) 227-1817. **Circle No. 533**

Novell Inc, Provo, UT, (801) 429-5900. **Circle No. 534**

Fluke transfers boundary-scan business to Dutch company

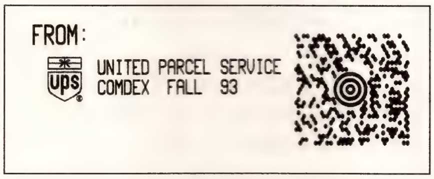
Fluke Corp has transferred its boundary-scan test business to a new Dutch company, JTAG Technologies BV. JTAG Technologies will now handle design, manufacture, marketing, sales, and postsales support of the boundary-scan products for current Fluke customers and new customers. Fluke retains the right to license the technology for use in its service-tools business.

JTAG Technologies comprises the staff that developed and marketed boundary-scan related products for Philips Test and Measurement, which Fluke acquired last May. The new company plans to focus on the market for supporting boundary-scan applications, such as testing, programming, and emulation.

The company has also entered into an exclusive contract for the development of boundary-scan products with Philips Research Laboratories in the Netherlands. Additionally, the newly formed company has made an agreement with Corelis Inc for Corelis to handle US sales of some JTAG Technologies' products. JTAG Technologies, in turn, will resell some Corelis products in Europe. The agreement also joins the two companies in mutual JTAG product development.—by Fran Granville

JTAG Technologies BV, Eindhoven, The Netherlands, 33-40-785104. **Circle No. 535**

Corelis Inc, Cerritos, CA, (310) 926-6727. **Circle No. 536**


FROM:
UNITED PARCEL SERVICE
COMDEX FALL 93

UPS unveils high-capacity code at Comdex

Technology sometimes springs from places where you least expect it. After years of research, the United Parcel Service (UPS) has perfected a 2-D, machine-readable printed code that offers far more capacity than do conventional bar codes. Called MaxiCode, the scheme encodes 100 characters into a 1-in.-square area. The code comprises a central target bull's eye surrounded by an array of hexagonal dots (**Fig 1**). UPS plans to put the code into the public domain. The company has also developed a CCD-based line-scan camera that scans MaxiCode labels on different-sized packages moving at 500 ft/sec, although the code suits any application that requires package tracking or inventory. UPS is looking for companies that would like to license the camera.—by Steven H Leibson

United Parcel Service, Danbury, CT, (203) 731-6399. **Circle No. 537**

Electronics maker moves factory to US shores

Raltron Electronics Corp has moved its quartz-crystal-oscillator facilities onshore to Miami. The reasons for the move are to provide direct factory sup-

SHORTS

ISO 9000 guidance. National Testing Systems has formed NTS Quality Services to address the need for practical advice for companies pursuing ISO 9000 compliance. NTS offers a wide range of services for military, aerospace, nuclear, automotive, and commercial quality standards. NTS Quality Services, Acton, MA, (508) 263-2933. **Circle No. 538**

European broadcaster licenses Intel video software. Paris-based TF1, Europe's largest private television broadcasting agency, has licensed Intel's Indeo video for the production of its first multimedia CD-ROM products. The Intel software allows for software-only video playback of Intel 486 and Pentium μP-based PCs. Indeo delivers "free" video playback to the desktop by eliminating the need for add-on hardware to play back video files. Intel Corp, Santa Clara, CA (408) 765-4483. **Circle No. 539**

Accel acquires Omation. Accel Technologies has acquired Omation, a manufacturer of PC-based design tools. Accel will continue to support Omation's Schema design tools and will soon contact users regarding support programs for Schema and upgrade options to Omation's Tango DOS and Tango-Pro for Windows. Accel will also provide file and library translators free to those customers wishing to make the transition. Accel Technologies, San Diego, CA, (619) 554-1000. **Circle No. 540**

Mentor acquires Checklogic. The acquisition of Checklogic, developer of automatic test-pattern-generation tools, strengthens Mentor Graphics' top-down ASIC-design technology in the design-for-test area. The acquisition evolved out of a partnership started in 1992 to develop test tools. Mentor Graphics, Wilsonville, OR. (800) 547-3000. **Circle No. 541**

SHORTS

Arrow sponsors European quality symposium. Arrow Electronics sponsored its first Pan-European quality symposium in Chantilly, France, in November. Approximately 200 executives and managers of leading semiconductor manufacturers and distributors, representing 13 countries, met to discuss quality-related issues. The participants also broached launching a formal European quality forum for collective discussions between manufacturers and distributors. The goal is to improve quality throughout the European electronics market. Arrow Electronics Inc, Melville, NY, (518) 391-1300. **Circle No. 542**

IEEE approves draft for compact embedded-PC modules. The IEEE P996.1 Working Group has approved a draft for IEEE ballot for standardizing compact embedded-PC modules. P996.1 chairman Rick Lehrbaum expects balloting to take six to 12 months. IEEE P996.1 Working Group Chairman, Sunnyvale, CA, (408) 522-3650. **Circle No. 543**

port, fast prototypes, and high-volume production deliveries for US manufacturers of host electronics products, says Alexander Wolloch, company president and chief executive officer. He says that when a crystal oscillator is made in Malaysia or Korea, it can be difficult for US engineers to call the factory for advice. Another disadvantage of offshore production is that prototype delivery can take 16 weeks or longer, notes Wolloch.—by Fran Granville

Raltron Electronics Corp, Miami, FL, (305) 593-6033. **Circle No. 544**

Testability-analysis and -synthesis tool speeds design

The DFTAdvisor tool from Mentor Graphics offers testability analysis, automated scan insertion, and design rule-checking capabilities. The tool helps ASIC designers evaluate designs for testability and identify problems early in the product-development cycle, before running automatic test-pattern generation tools. Once the tool identifies problems, you can use the test-synthesis capability to insert scan and test logic structures to improve the design's testability. Mentor Graphics has integrated DFTAdvisor into its design tools, and you can also use it as a point tool with other design tools such as Synopsys' Design Compiler. DFTAdvisor is available now and starts at $20,000 for a floating license.—by Doug Conner

Mentor Graphics, Wilsonville, OR. (800) 547-3000. **Circle No. 545**

Researchers boost speed of P-channel MOSFET

Researchers at Cornell University have developed a transistor that boosts the speed of a P-channel MOSFET (metal oxide semiconductor field-effect transistor) by as much as 40%. The speed boost allows a P-channel device to match the speed of an N-channel device.

The Cornell researchers (Yosef Shacham-Diamand and Kaushik Bhaumik) used a 100-Å layer of silicon-germanium to create a quantum well. The well captures holes and gives them a faster conduction path that has less resistance than available in previous P-channel devices. Test devices switched at 35 GHz and produced 5 mA at 1.5V.—by Richard A Quinnell

Cornell University, Ithaca, NY, (607) 255-1548. **Circle No. 546**

IEEE agrees on foundation media-access control for wireless LANs

The IEEE 802.11 committee for wireless LANs voted at its November meeting to base the forthcoming standard media-access-control protocol on a proposal submitted by NCR Corp, Symbol Technologies, and Xircom Inc. The standard's goal is to ensure the interoperability of wireless LANs from different manufcturers and for use with a variety of physical layers, such as direct sequence or frequency hopping, spread-spectrum radio, and IR. The foundation access method is based on the Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA).

Companies supporting the proposal include Advanced Micro Devices, AT&T Global Business Communications Systems, ICL Retail Systems, National Semiconductor Inc, NEC Corp, Norand Corp, Telxon Corp, and Toshiba America Information Systems.

The equipment that implements the protocol supports ad-hoc and infrastructure peer-to-peer wireless LANs. The protocol allows infrastructure LANs to be interconnected via an access point wih a wired network. Use of the protocol enables mobile users to roam throughout a facility while maintaining continuous connenction to network resources.—by Fran Granville

NCR Corp, Dayton, OH, (513) 445-5236. **Circle No. 547**

Symbol Technologies, Bohemia, NY, (516) 244-4191. **Circle No. 548**

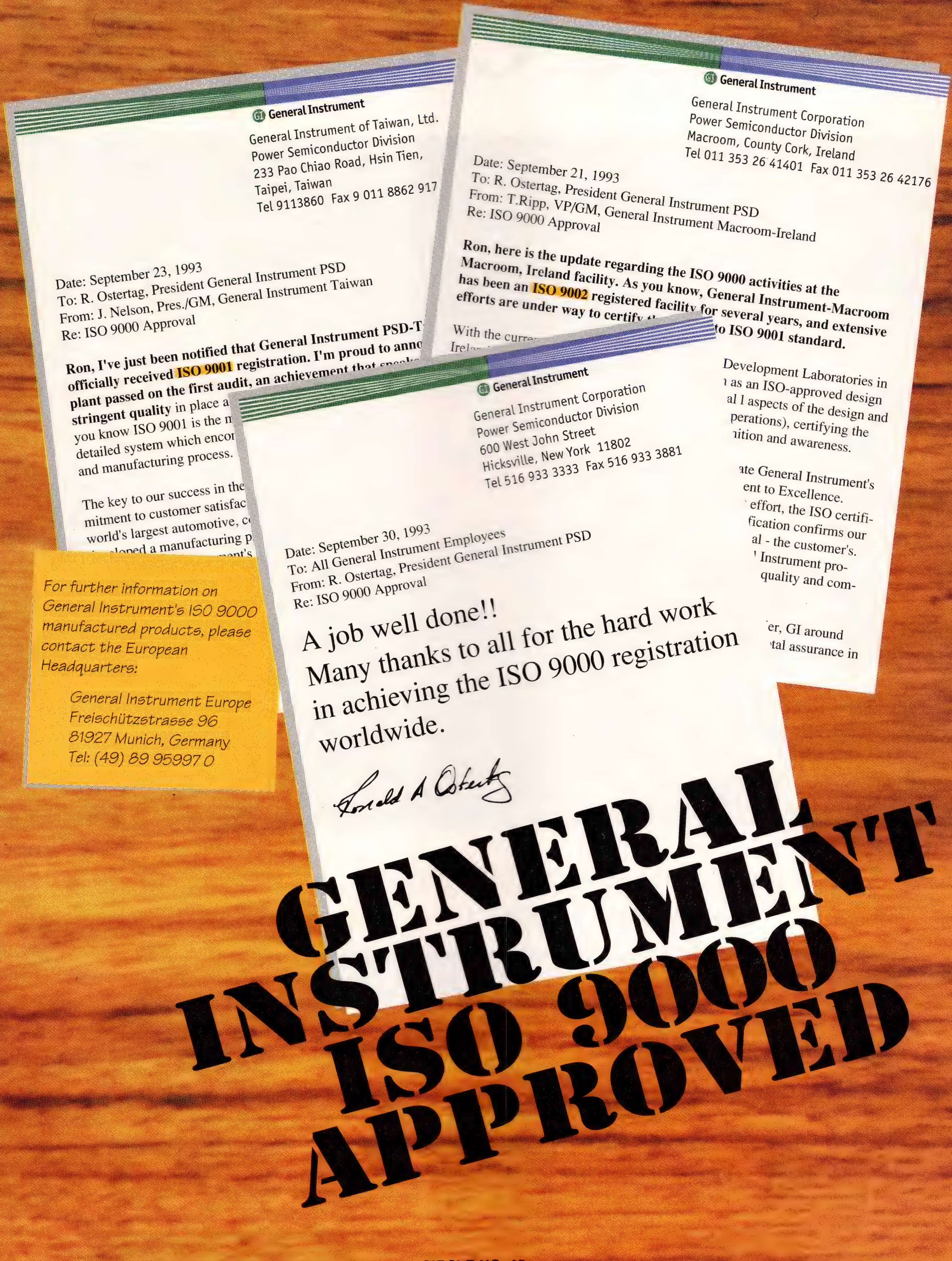
Xircom Inc, Calabasas, CA, (818) 878-7600. **Circle No. 549**

DSO takes 1 Gsamples/sec in real time on two channels at once

Deja vu? Not quite. The past 12 months have seen quite a few introductions of DSOs that offer attractive features at prices below $5000. As *EDN* has repeatedly pointed out, each new model offers something different. Tektronix's 2-channel, 200-MHz-bandwidth TDS 350 ($3995, including passive probes) is the first under-$5000 DSO to acquire waveforms on two channels simultaneously at 1 Gsamples/sec. To sample any faster, you need one of the DSOs we covered in our July 8, 1993, issue. Those cost three to four times as much.

Like its lower speed siblings (the $2795, 100-MHz-bandwidth TDS 320 and the new $2295, 50-MHz-bandwidth TDS 310), the TDS 350 offers a choice of acquisition modes. Among them is peak-detect mode, operable from 25 µsec/div to 2.5 sec/div. This mode eliminates aliasing and, even at 2.5 sec/div, captures glitches as brief as 10 nsec. Another mode effectively reduces noise by averaging waveforms over multiple acquisitions. The scopes also offer a choice of waveform displays, including vector accumulation, which highlights the most recently acquired waveform in bright vectors against a background of all waveforms captured over a user-defined interval.—by Dan Strassberg

Tektronix Inc, Beaverton, OR, (800) 426-2200. **Circle No. 550**



General Instrument

General Instrument of Taiwan, Ltd.
Power Semiconductor Division
233 Pao Chiao Road, Hsin Tien,
Taipei, Taiwan
Tel 9113860 Fax 9 011 8862 917

Date: September 23, 1993
To: R. Ostertag, President General Instrument PSD
From: J. Nelson, Pres./GM, General Instrument Taiwan
Re: ISO 9000 Approval

Ron, I've just been notified that General Instrument PSD-T
officially received ISO 9001 registration. I'm proud to anno
plant passed on the first audit, an achievement that speaks
stringent quality in place a
you know ISO 9001 is the m
detailed system which encor
and manufacturing process.

The key to our success in the
mitment to customer satisfac
world's largest automotive, c
developed a manufacturing p

General Instrument

General Instrument Corporation
Power Semiconductor Division
Macroom, County Cork, Ireland
Tel 011 353 26 41401 Fax 011 353 26 42176

Date: September 21, 1993
To: R. Ostertag, President General Instrument PSD
From: T.Ripp, VP/GM, General Instrument Macroom-Ireland
Re: ISO 9000 Approval

Ron, here is the update regarding the ISO 9000 activities at the Macroom, Ireland facility. As you know, General Instrument-Macroom has been an ISO 9002 registered facility for several years, and extensive efforts are under way to certify
to ISO 9001 standard.

With the curre
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Development Laboratories in
as an ISO-approved design
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effort, the ISO certifi-
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Instrument pro-
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General Instrument

General Instrument Corporation
Power Semiconductor Division
600 West John Street
Hicksville, New York 11802
Tel 516 933 3333 Fax 516 933 3881

Date: September 30, 1993
To: All General Instrument Employees
From: R. Ostertag, President General Instrument PSD
Re: ISO 9000 Approval

A job well done!!
Many thanks to all for the hard work
in achieving the ISO 9000 registration
worldwide.

Ronald A Ostertag

For further information on General Instrument's ISO 9000 manufactured products, please contact the European Headquarters:

General Instrument Europe
Freischützstrasse 96
81927 Munich, Germany
Tel: (49) 89 95997 0

GENERAL INSTRUMENT ISO 9000 APPROVED

CIRCLE NO. 48

Imagine it got 300

Get maximum performance on a minimum of power.

NATIONAL'S 3V ANALOG

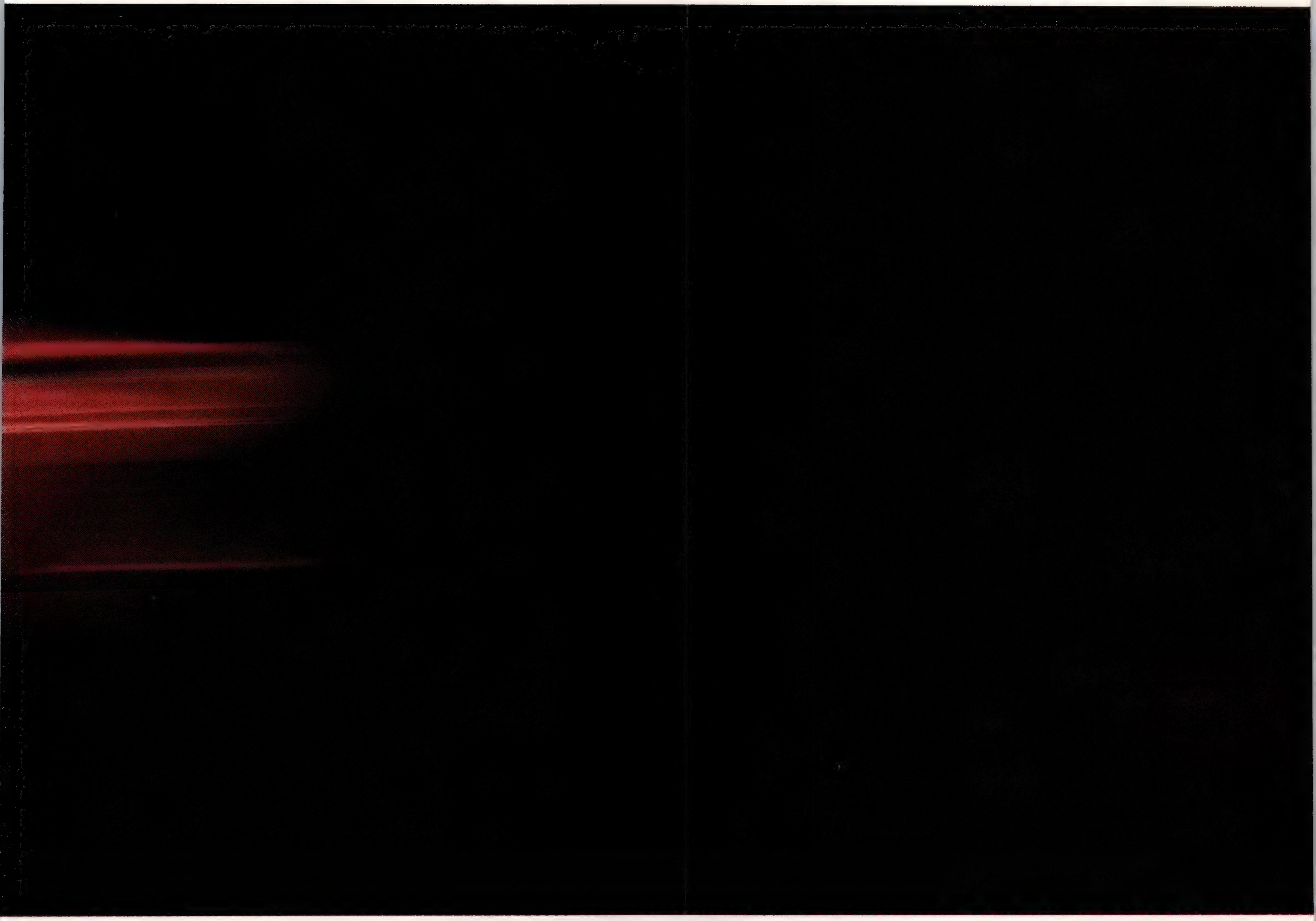
Envision yourself pushing high-performance to the absolute limit, without the slightest regard for fuel consumption.

It's more than just a figment of your imagination. It's 3V analog from National, a portfolio of analog ICs designed to offer 3-volt operation without sacrificing performance.

It's the LM12L454/8, a single-chip data acquisition system that features 106ksps throughput and 15mW (max) power dissipation. Or the LMC6482/4, an op amp that offers rail-to-rail

Part #	**Model**
LM12L454/8	12-Bit Plus Sign Data Acquisition System
ADC12L030/2/4/8	12-Bit Plus Sign A/D
LMC6572/4	Op Amp
LMC6482/4	Op Amp
LM2574/75/76	SIMPLE SWITCHER™ Power Converter
LP2950/51	Low Dropout Regulator
LM4041	Voltage Reference

miles per gallon.



Performance Package

- System on a chip with 106ksps throughput and 15mW (max) Pd
- Fastest 3V 12-bit serial A/D at 15mW (max) Pd (40µW in powerdown)
- Low power (40µA/op amp) Guaranteed 2.7V operation
- Rail-to-rail input and output at 3V
- First easy-to-use power converter family with 3.3V output and guaranteed system performance
- Very low dropout voltage (380mV) and quiescent current (75µA)
- Subminiature SOT-23 packaging with adjustable voltage option (1.24V to 10V)

input and output at 3V. Or the LP2950/51 low dropout voltage regulator, which provides extremely low dropout voltage (380mV) and quiescent current (75µA).

In fact, our 3V family includes a full range of data acquisition, power management, and amplifier ICs. All of them are designed to increase the performance of your portable designs—while reducing power consumption. And all of them come with the quality and reliability you expect from a world leader in analog technology.

For product samples and data sheets, call us at **1-800-NAT-SEMI, Ext. 267**. And we'll fuel your imagination with 3V analog.

National Semiconductor

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WIRELESS

DESIGN SOLUTIONS

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Focusing On The Issues

Portable Communications Products

With the demand for integrated data, graphics, voice and video transmission capabilities, designing products for the subscriber side of wireless will require IC-level products with wide data bandwidths, low power, CODEC capabilities and extremely high on-chip integration. And because of user location and wireless infrastructure limitations, satellite uplink capabilities will be required.

Infrastructure

As the number of wireless users continues to grow, so also will the demand for seamless communications capabilities regardless of user location. This may require the development of multiple close-range microcells (<a few hundred meters) deployed around fast and flexible macrocell base stations. These base stations will need a great deal of computing power, bandwidth and software-driven intelligence.

Distribution

In 1993, the U.S. FCC allocated portions of the 2GHz and 900MHz bands of the electromagnetic spectrum for PCS and narrowband PCS respectively. As spectrum allocation and usage continues, users will benefit from new, lower-cost services.

©1994 Mitsubishi Electronics America Inc., Electronic Device Group, Sunnyvale, California

Across The Spectrum.

Wireless technology is permeating business and personal communications globally, driving portable product size and performance to totally new levels.

For OEMs, this means designing products that can operate across the spectrum. It means integrating more functions into single-chip solutions so that more features and applications can be designed into smaller and lower-power end products.

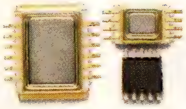
Mitsubishi has already begun RF integration onto single-chip GaAs MMICs for PCS applications, replacing 10 to 12 discrete components with a single, 3.4V transmitter device. We developed battery recharge ICs with 10-bit A/D accuracy and on-chip DSP; PLLs with on-board prescalers; and highly-integrated MCUs with 48KB ROM, 2KB RAM, I/O and a dot-matrix LCD controller on chip.

For microcell base station applications, Mitsubishi has integrated a laser diode, transmitter, receiver and support circuitry into a single, plug-and-play transceiver device.

Mitsubishi has also addressed the single-chip challenge by developing synchrotron-based production facilities to drive submicron silicon technology to the 0.25µm level and lower.

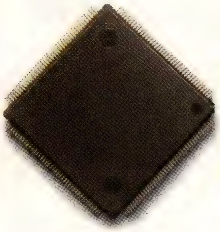
For more information on the wide range of Mitsubishi products for wireless, and to receive a free wall chart, *Guide to ICs and Components for Wireless Applications*, call **1-(800)-886-4088**

PRODUCT	Cordless/Cellular Phones (Analog & Digital)	Portable Storage	Mobile PCs/Terminals	Battery Monitor Control	PCN/PCS, WLANs, PDAs	Microcells	Wireless PBX	Global Positioning	FEATURES
Low-voltage Baseband ICs	◆								On-board Scrambler, Compander, Modem
Battery Recharge ICs	◆								10-Bit A/D Accuracy; On-chip DSP
PLL ICs	◆		◆		◆		◆	◆	Dual PLL Frequency Synthesizers
Voltage Detect & Reset ICs	◆								1.25V or 4.25V Detection
RF Power Amplifiers	◆		◆		◆	◆	◆		High Efficiency, Low Voltage, Surface Mount, Small Package
RF Switches	◆		◆		◆	◆	◆		Low Insertion Loss, Surface Mount
HEMT Devices								◆	High Gain, Low Noise, Surface Mount
Fiber Optic Base Station Transceiver						◆			900 MHz; Plug-and-play; Eliminates RF Blackout Areas
16-Bit MCUs	◆	◆	◆				◆		Up to 48KB ROM/2KB RAM or ROM-less, Very Low Power (4mA at 8MHz), Small Package
8-Bit MCUs	◆		◆	◆	◆				Up to 48KB ROM, On-chip Dot-matrix LCD Controller, 2.5V Operation
0.8µm Gate Arrays	◆		◆	◆	◆	◆	◆	◆	6K-250K Usable Gates, Clock Rates to 100MHz, 215 psec Delay, Low Power
Low-voltage DRAMs (4M/16M)		◆	◆		◆		◆	◆	3.3V, Self Refresh, Byte-wide
Low-voltage Cached DRAMs (256K x16)		◆	◆		◆		◆	◆	3.3V, Self Refresh, Byte-wide
Slow SRAMs	◆		◆		◆		◆		For Low-power, Battery-operated Data Storage
Flash Memories	◆	◆	◆		◆		◆		On-board Reprogrammability; For Code Storage, Data Storage,BIOS
EPROMs/OTP ROMs	◆	◆	◆		◆		◆	◆	Low Voltage, CLCC/TSOP Package
I/O Cards	◆		◆		◆			◆	Fax/Modem, LAN
Memory Cards	◆	◆	◆		◆			◆	DRAM, SRAM, Flash, Mask ROM

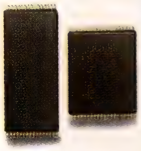


RF & Microwave Devices

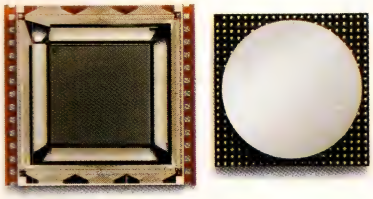
3.3V DRAMs with enhanced power management for "green" projects



Mitsubishi MCU with on-board dot matrix LCD controller



1M & 4M Flash memories (x8, x16)



0.8µm CMOS gate arrays and embedded cell arrays, up to 400,000 gates

Smart battery recharge ICs

PCMCIA/JEDEC standard and custom memory cards

CIRCLE NO. 49

MITSUBISHI

Let us guide you through the bar code jungle.

You're never alone when you choose to enhance your system with HP's complete family of bar code components.

It's a jungle out there. With the increasing levels of competition in the European marketplace, it takes genuine added value to stand out.

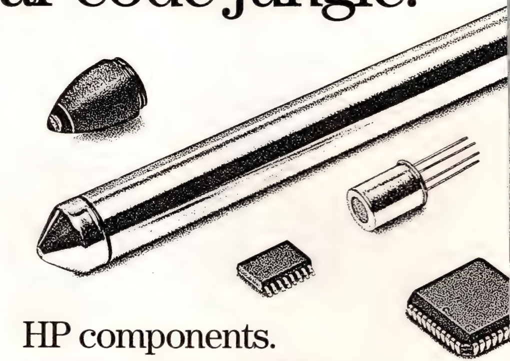
Now, thanks to HP, adding bar code scanning and data entry ability to your product is a simple and cost-effective way to enhance its value. HP has always been a leader in contact scanning bar code technology. And today, we offer a complete, reliable, and flexible family of bar code components.

Our products lead the way.

With our guidance, the path to bar code is very simple. HP's complete line of products include everything you need — a choice of reflective sensors, integrated digitizer ICs, sapphire tips, a family of single chip decoder ICs, and a broad range of wands. Including our new stainless steel tube.

With so many choices, it's easy to assemble a bar code system that works with your application — with little impact on the cost or size.

You'll find it's an idea well worth exploring. In Europe, begin by faxing your request for more information to 31 2503 52977.



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CIRCLE NO. 65

Errata

We erred in our *Microprocessor Directory* review of Intel's MCS-96 16-bit μC (EDN, November 25, 1993, pg 114). Intel is not the only vendor. The **OVERVIEW** should include a second paragraph:

Two other companies also make 196s. AT&T Microelectronics sells a 196 CPU core in its cell libraries for ASICs; IBM Microelectronics now sells 196 chips, which previously were used in IBM products (IBM MC196xx chips are basically core 196s with a few peripherals).

The **VENDORS/PRICING** section should include IBM pricing: MC19610 (20 MHz, 32-kbyte ROM, 1-kbyte RAM, 2-bit ADC, 80-pin PFP), $17; MC19611 (20 MHz, 4-kbyte ROM, 1-kbyte RAM, 80-lead PFP), $14; MC19620 (33 MHz, 1-kbyte RAM, 10-bit ADC, 100-lead PFP), $20.

In addition, the Intel i960 writeup (pg 154) is incorrect. We identified the chip as a microcontroller; the i960 is a microprocessor. The **OVERVIEW** section should have no second paragraph. The **VENDORS/PRICING** section should read: Intel is the developer and sole supplier. 16-MHz i960SA, $15.90 (plastic); 16-MHz i960KA, $21.35 (plastic); 25-MHz i960CA, $91.90 (plastic); 33-MHz i960CA, $120.60 (ceramic PGA); 25-MHz i960CF, $137.70; 33-MHz i960CF, $180.75 (ceramic PGA) (1000).

We regret the error .

Don't forget about aliasing

Thank you for warning unwary test engineers and scientists about the effects of "common enemy number one—electrical noise" in Brian Kerridge's "Plug-in data-acquisition boards transcend noisy environments" (EDN, October 28, 1993, pg 47). Noise from the electrically unfriendly PC Bus has been a real problem for board-level designers, especially now, as 33- and 66-MHz processors become standard.

Some users have tried sampling "above" noise levels and then digitally filtering data as an easy way to eliminate this problem. But, sampling at 100 kHz when the bandwidth is only 20 kHz or less is inefficient: The high-speed board is very expensive, and excess data must be absorbed.

In addition, noise frequencies extend well beyond the sampling rates of current A/D converters. Aliased high-frequency components can "fold back" and appear as lower frequencies that cannot be distinguished from valid sampled data. Users may not know if these aliasing or false errors are obscuring real events and may increase sampling rates even though the aliasing phenomenon occurs independently of conversion speed.

The best way to ensure data integrity is to filter noise properly from the signals with an antialias filter board, which prevents high-frequency input signals from folding over into the lower frequency region of the discrete signal. Such a board, including the AAF-1 filter board from Alligator Technologies, is ideal for any instrumentation system with a sensor and a monitoring computer. It often can filter two or more differential or single-ended channels and may be compatible with data-acquisition boards from manufacturers such as Keithley, Data Translation, and National Instruments.

Greg Gangitano
Sr Applications Engineer
Alligator Technologies
Fountain Valley, CA

(Editor's note: Aliasing is another source of system error, and Gangitano is quite right to remind us of possible effects. Readers should remember, though, that PC plug-ins provide primarily a low-cost route to data logging. The card Gangitano recommends costs $851 (two channels). For a typical system with eight channels, you'll pay more for a filter card than for the data-acquisition card alone.

An application note on how to eliminate aliasing errors in A/D conversion is available from Alligator Technologies, 17150 Newhope St, Suite 114, Fountain Valley, CA 92728, USA.)

Send your letters to Signals and Noise Editor, EDN, 275 Washington St, Newton, MA 02158. Or fax us at (617) 558-4470. EDN reserves the right to edit letters for clarity and length.

No ghost writers here...

Due to an oversight, a byline for Technical Editor Ray Weiss, EDN's μP guru, was not typeset in our 20th Annual Microprocessor and Microcontroller Directory (EDN, November 25, 1993, pg 59).

Ray Weiss is your primary technical contact and resource for μP and μC coverage at EDN. You can reach Ray's office (Woodland Hills, CA) at (818) 704-9454, fax (818) 704-7083.

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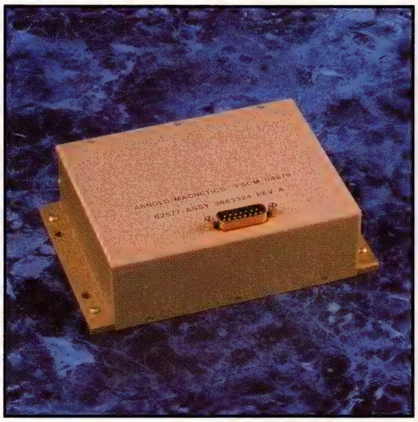

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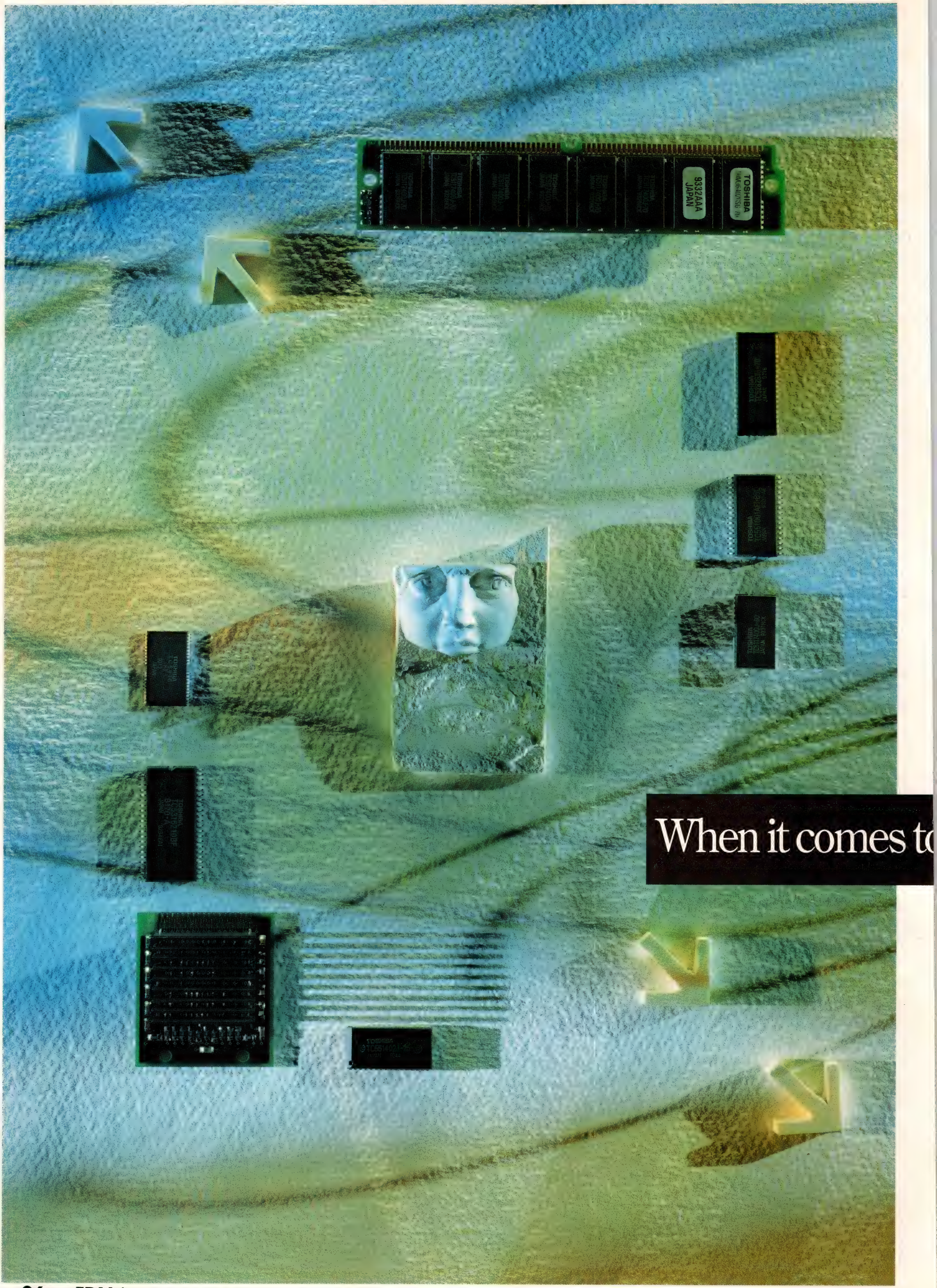
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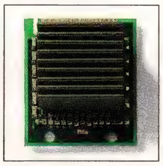

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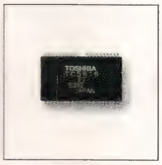

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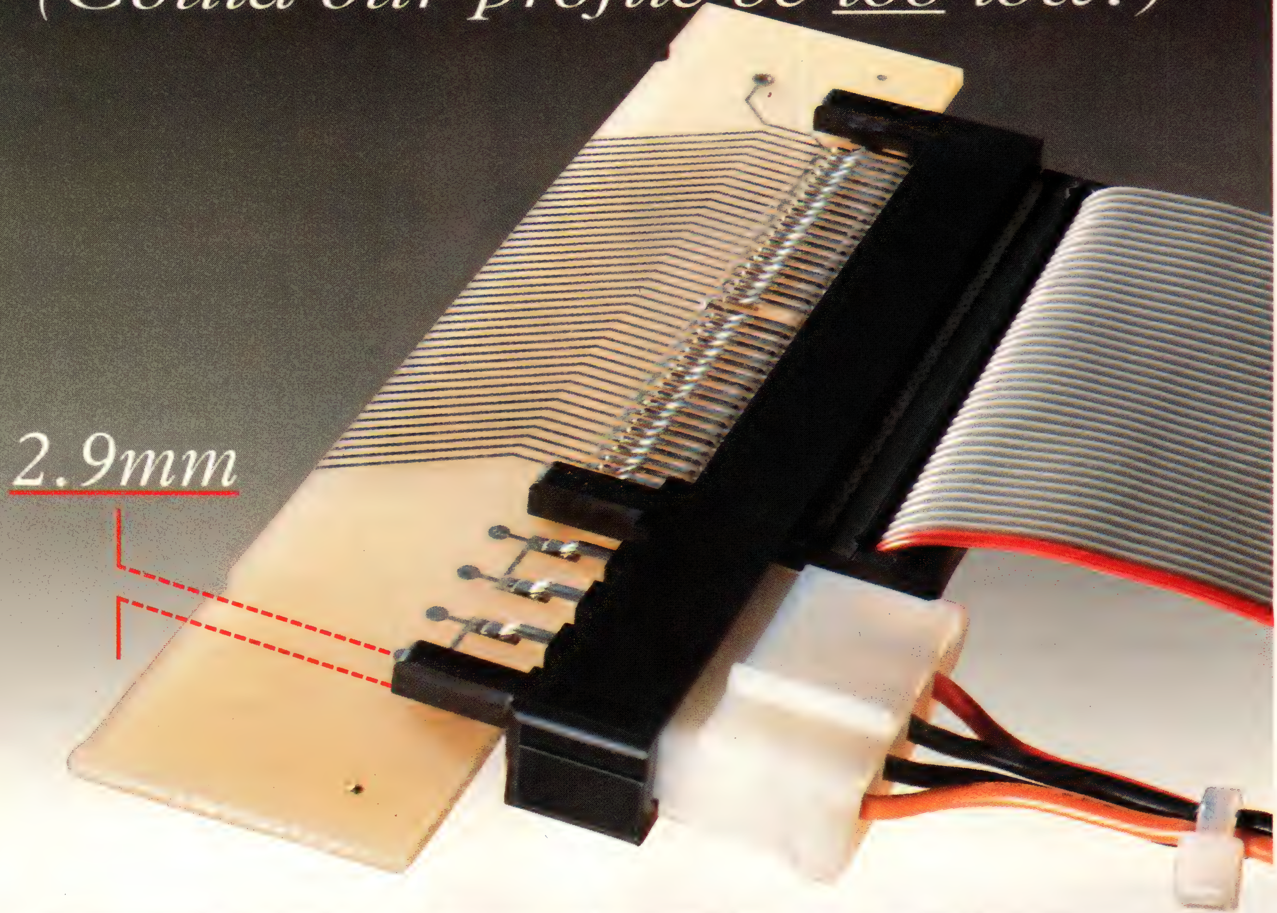

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CIRCLE NO. 70

Ask EDN

EDITED BY JAMES P LEONARD

Fruitless search in the plain of Spain

I work in Madrid and am searching for a double-matched JFET device from National Semiconductor (part 2N5565). Unfortunately, this model has never been distributed in Spain, and National doesn't sell this part in quantity of less than $3000 worth of JFETs. Any suggestions of other component suppliers in the United States—or abroad—that sell in small quantities?
Javier Guadalajara
Madrid, España

First, contact:
Digi-Key
701 Brooks Ave S, Box 677
Thief River Falls, MN 56701, USA
(800) 344-4539
Fax (218) 681-3380.

Digi-Key stocks National transistors, but not specifically the 5565; however, Philips BFQ10 through 16 are equivalents. In addition, Central Semiconductor (Hauppauge, NY, (516) 435-1110), Crimson Semiconductor (New York, NY, (212) 947-8585), and Diode Transistor Co Inc (West Caldwell, NJ, (908) 686-0400) are alternate sources.

A helpful contributor to the *EDN* bulletin-board-system has a couple of suggestions, too. Siliconix has European distributor representatives in Madrid:
Comercial Española de Componentes SA
Arzobispo Morcillo
24 Oficina 5
Madrid 28029
(1) 733-7054
Redis Logar SA
Lopez de Hoyos
78 DPDO
Madrid 28002
(1) 411-3561

Also, try using some more common parts, such as 2N5545 or 2N3955A, which have ECG equivalents of ECG461.

Eagle eye's interest piqued

I have always respected *EDN* for its accuracy in spelling, abbreviations, and capitalization in typesetting engineering units. However, I noticed in Gary Legg's "Small, rugged disk drives take (fairly) hard knocks" (EDN, November 11, 1993, pg 41) a consistent use of uppercase "G" to represent acceleration of gravity. I often see this in print as lowercase "g." I haven't cracked a physics book in 36 years. Which is correct?
Wayne E Hough
Kryptos Corp
Mukilteo, WA

Most sources prefer the lowercase "g" for abbreviating the force of gravity, but it's also the abbreviation for grams. So, when you write about a lightweight, shock-resistant disk drive, it can get confusing. That's why we used "G" for gravity in the article, even though it was inconsistent with our editorial style; usually, we set "g" in lowercase.

Pan-Atlantic search for parts

I'm designing a rather unusual and nonstandard audio application, for which I need to use a low-cost electret microphone cap. Many such devices are available on the market, with and without internal preamplifier/buffer, but none of the distributors I've contacted can provide sufficiently detailed technical information (for instance, frequency response vs dc polarization current, environmental restrictions, etc) or provide a manufacturer name.

Therefore, I'm searching for detailed data sheets containing full specs and application information for both a basic electret cap and a preamplified version of it.
Dr Paolo Zambusi
Società Italiana
Controlli e Collaudi Srl
Selvazzano Dentro, Italia

Begin by contacting *Electronics World/Wireless World*, Quadrant House, The Quadrant, Sutton, Surrey SM2 5AS, UK, (081) 652-3128, fax (081) 652-8956. The staff may be able to put you in touch with a manufacturer of your required parts. If possible, also try the Madisound electronic bulletin-board service in the United States at (608) 836-9473; perhaps another user has some information.

Is such a device within reach?

I am searching for literature on a passive-triggering device (ie, a small magnet) that is proximity-detection sensitive to at least 12 in.; heat, light, and sound means are not practical.
Michel Masse
Woodland Hills, CA

Senior Technical Editor Charles Small replies: Finding the proper sensor depends heavily on what your application senses, its environment, and the output desired. For a start, contact the following companies:
RDP Electrosense
RD 2, Route 100
Pottstown, PA 19464
(215) 469-0850
Kaman Instrumentation Corp
1500 Garden of the Gods Rd
Box 7463
Colorado Springs, CO 80933
(719) 599-1500
Gordon Products Inc
Del Mar Dr
Brookfield, CT 06804
(203) 775-4501.

OTP chips aren't recyclable

You cannot erase one-time-programmable (OTP) memory or microcomputer chips with UV light because their EEPROM cells are encased in opaque plastic. Is it possible to erase them by using x-ray exposure? If so, what dosage is necessary and what secondary damage would the IC experience after x-ray exposure?
Raymond Weisling
Solo, Indonesia

Technical Editor Richard Quinnell responds: Do not try using x-rays for erasing: The necessary x-ray dosage would damage the oxide layer of the device. If you need to make only small changes, try changing the 1s to 0s—but remember that you cannot change 0s to 1s.

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Acknowledging engineers' visual intelligence

The history of technology and the new field of cognitive psychology both have vital lessons to impart to engineering. Yet no one developing software tools for hardware or software seems to be aware of either the history of technology or cognitive psychology.

New theories about human intelligence illuminate why engineers cannot explain anything without drawing diagrams—why some people feel instantly at home with diagrammatic programming and some do not. (See **Special Report**, "Diagrammatic Programming," pg 60.) Why a messianic zeal inflames some people to inflict "hardware-descriptions languages" on engineers.

Most of us lack the vocabulary to even begin discussing the subject. As noted researcher Howard Gardner points out (**Ref 1**), "intelligence" has a very limited meaning in Western culture. To Westerners, an "intelligent" person is quick-witted, wise, and rational. Other qualities are not recognized as "intelligence."

Gardner postulates multiple intelligences. His theory of multiple intelligences is essential to understanding the chasm that separates visual from textual design methods and their respective practitioners from each other.

Science has bolstered Gardner's theory because computerized brains scans reveal that people use separate areas of their brains for visual and textual tasks.

Mathematical, musical, and language abilities all meet Gardner's criteria as separable intelligences. Less well known, but just as easy to demonstrate as these abilities, is visual intelligence. And visual intelligence is the key to the power of diagrammatic programming.

Everyone knows that engineers typically rank in the upper few percentiles in mathematical ability. Less well known is that engineers rank in those same lofty percentiles in visual intelligence. Alas, visual and literary ability seldom go hand in hand. Engineers rank in the 30th percentile or lower in language ability.

Engineers think and express themselves visually. Engineers' tools and methods require no words. Engineers' extraordinary visual intelligence allows them to create designs and solve problems in ways that no computer can duplicate and, unfortunately, in ways that many nonengineers cannot appreciate. No words can express how the power, beauty, and elegance of a good design stirs the passion of an engineer.

Thomas G West (**Ref 2**) documents the correlation between extraordinary visual intelligence and mild to severe dyslexia. In other words, engineers are singularly unsuited to text-based tools.

Henry Petroski's *The Pencil* (**Ref 3**) is a historical look at technologists.Using pencils, technologists have always produced a drawing of what a device is, not a textual description of what it does.

Petroski is a civil engineer and is thus perhaps unaware that the scribblers do control one technological area: programming.

Professor Eugene S Ferguson (**Ref 4**) further expands upon Petroski's point that technology is a mixture of science and art by decrying the emphasis in engineering education on theory at the total expense of practice. Ferguson further demolishes the idea of top-down—a method that text-based tool proponents universally endorse.

Experienced technologists, no matter what their fields, would never advocate top-down design. Yet, revealingly, proponents of text-based tools, such as VHDL, and object-oriented programming, reveal their lack of understanding of how visually oriented engineers really work by championing top-down design.

Charles H Small
Senior Technical Editor

References

1. Gardner, Howard, *Frames of Mind, the Theory of Multiple Intelligences*, Basic Books, New York, NY, 1985, ISBN 0-465-02508-0.

2. West, Thomas G, *The Mind's Eye*, Prometheus Books, Buffalo, NY, 1991.

3. Petroski, Henry, *The Pencil*, Alfred A Knopf, New York, NY, 1990.

4. Ferguson, Eugene S, *Engineering and the Mind's Eye*, MIT Press, Cambridge, MA, 1993.

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July 1993
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PC Magazine
July 1993

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CIRCLE NO. 72

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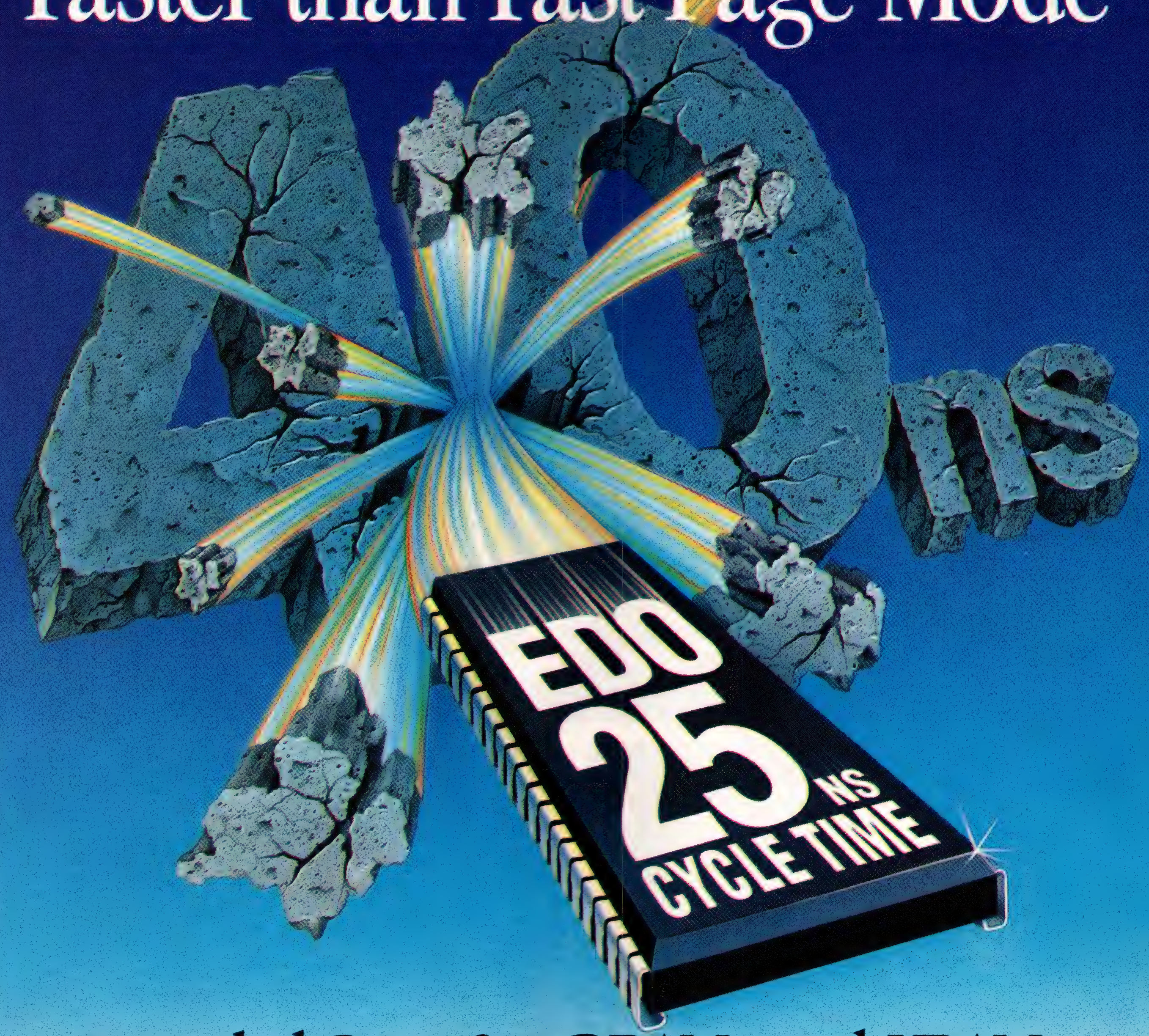

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MT4LC4007J	4 Meg	1 Meg x 4	60/25, 70/30	Now/2Q94
MT4C16270	4 Meg	256K x 16	60/25, 70/30	Now
VRAMs				
MT42C256K16A1	4 Meg	256K x 16	60/24, 70/27	Now
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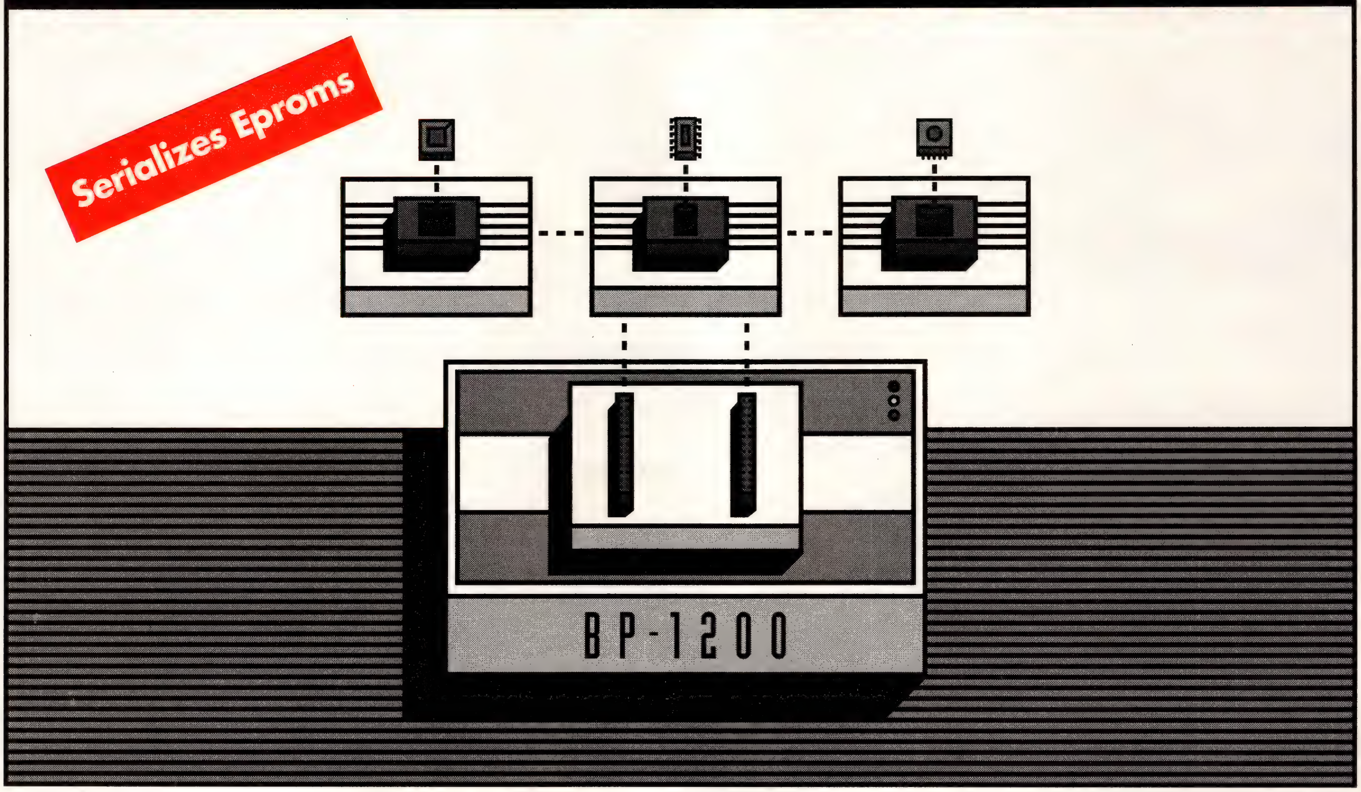

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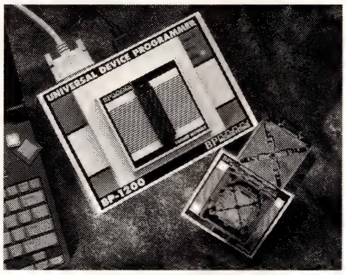

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*Only on BP-1200s purchased in the U.S. after September 15, 1993. Some restrictions and exclusions apply. Features and specifications subject to change without notice. Call for details.

CIRCLE NO. 74

FAST ETHERNET

Emerging 100-Mbit Ethernet standards ease system bottlenecks

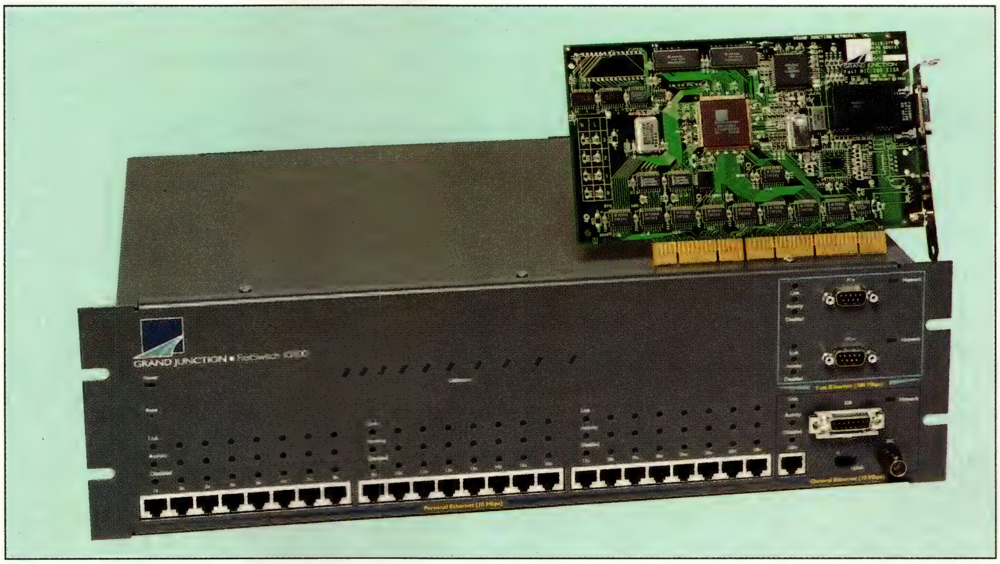
RICHARD A QUINNELL, Technical Editor

The networking industry is developing faster versions of Ethernet to meet increasing demands for LAN capacity. As a result, two standards are now emerging—each reflecting a different cost or capability tradeoff.

Although a 10-Mbps data rate seemed generous when Ethernet first appeared, today's network users increasingly view it as inadequate. As a result, IC and local-area-network (LAN) system vendors are rushing to define a faster Ethernet, one that runs at 100 Mbps. Two distinct IEEE standards for a fast Ethernet are emerging, but neither is fully developed. Some companies, however, have already released their own versions of 100-Mbps Ethernet.

The need for a faster Ethernet results from the combination of two factors: increasing numbers of network users and increasing user-bandwidth needs. The increasing number of users implies that the average bandwidth available to each user in a shared network is decreasing (**Fig 1**). According to estimates from market-research firm International Data Corp (IDC), the average number of users per network segment will increase from 12 in 1991 to 21 in 1994. The average bandwidth available to each user thus drops more than 40%.

As available bandwidth is dropping, each user's bandwidth demand is increasing. The growth in processing power at each node, combined with the corresponding growth in data-transfer needs, boosts bandwidth demands of current applications. In addition, emerging data-intensive applications, such as video conferencing, contribute to the trend. These applications are time critical, which further complicates network needs. Audio and (to a lesser extent) video must be transmitted within a set period or they become impossible to reconstruct properly at the receiving end. If the network is crowded, conventional shared Ethernet cannot guarantee the timely network access such applications require.



Offering both 10BaseT and 100 Base-X Ethernet ports, the FastSwitch 10/100 represents the first step toward a 100-Mbps Ethernet network. The device serves as a 10BaseT switching hub with a high-speed link to an EISA bus server.

EDN's computer bulletin-board system (BBS) has a demo version of Dimension International's Superscape virtual-reality software. Phone (617) +558-4241 with modem settings 300/1200/2400 8,N,1. Access */freeware* SIG and specify *(r)ead* option followed by *(k)eyword* search for "TU #398".

FAST ETHERNET

Guaranteed access was one of several technical goals developers considered when choosing an approach to fast Ethernet. A second requirement was to use unshielded twisted-pair (UTP) wire for cabling—with as few pairs as possible. And a third goal was to limit the frequency content of signals along the UTP to 30 MHz to avoid FCC (Federal Communications Commission) Class A compliance testing.

Yet marketing—not technical—goals ultimately dictated the proposals vendors set before the IEEE 802 standards committee. Two markedly different proposals, representing distinct market views, have now reached draft-proposal stage: 100 Base-X and 100 Base-VG. Because these proposals serve different customer needs, the IEEE 802 committee decided (in November, 1993) that both would be refined into standards. The committee slated the 100 Base-X proposal to become standard 802.3U and the 100 Base-VG proposal as 802.12. **Table 1** compares the two proposals.

A collection of networking product vendors known as the Fast Ethernet Alliance (see **Table 2**) spearheads the 802.3U, or 100 Base-X, proposal. Alliance members aim to leverage existing Ethernet system software and hardware to reduce the cost and risk of upgrading a system to fast Ethernet. Their proposal, therefore, calls for retention of Ethernet's present media-access-control (MAC) layer protocol.

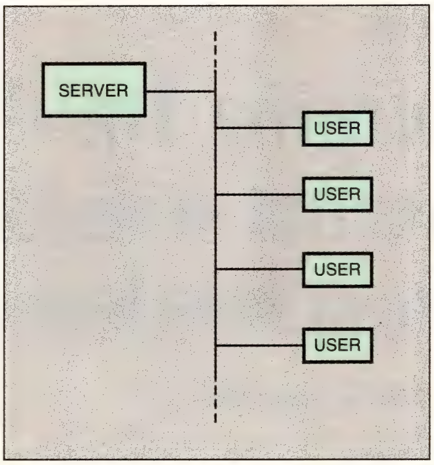


Fig 1—Conventional Ethernet has many users sharing the same bus. The bandwidth available to each user, on the average, decreases as users increase.

The protocol, named CSMA/CD (carrier sense multiple access with collision detection), requires that nodes desiring network access first listen to the network to determine if it's in use. If the network is free, the node may begin transmitting but continues to listen to detect any collisions—simultaneous transmissions by two or more nodes. If a collision occurs, the CSMA/CD protocol calls for the contending nodes to cease transmission and try again following a randomly timed delay. If several collisions occur in succession, the nodes double their delay interval and keep trying.

Although the CSMA/CD protocol eventually allows one node to gain access, the delay between access request and acquisition is both variable and unbounded. Further, a heavily loaded network spends considerable time resolving collisions, which is known as thrashing. Thrashing causes available network bandwidth to drop well below the 10-Mbps data rate; by some estimates, as much as 40% of system bandwidth may be lost.

100 Base-VG guarantees access

The 100 Base-VG proposal, which originates from industry giants Hewlett-Packard, IBM, and AT&T, seeks to avoid thrashing and to offer guaranteed network access by operating with a demand-priority protocol at the MAC layer. This deviation from CSMA/CD means that 100 Base-VG is not strictly an Ethernet variant; it is, however, a fast-Ethernet alternative, because it handles Ethernet data frames. 100 Base-VG also handles token-ring frames, thus providing an upgrade path for both Ethernet and token-ring users.

The demand-priority protocol of 100 Base-VG calls for the network hub to arbitrate network-access requests based on round-robin polling. The result is full utilization of network bandwidth. The hub polls for port-access requests, creates a requester list, then grants access to ports in the list order. Each requesting port gets a turn before the poll is taken again.

The demand-priority protocol also provides high-priority access, allowing a port to receive access ahead of its normal turn. Round-robin polling also determines high-priority request handling and requires that all high-priority users be serviced before normal-priority users gain access. Normal-priority users cannot be locked out, however. If a normal-priority access request has been pending for more than 250 msec, the hub automatically upgrades that request's priority status so that it is serviced in the high-priority sequence.

Choose 2- or 4-wire

Along with their protocol differences at the MAC layer, the two fast-Ethernet proposals differ in their physical layer. The 100 Base-X proposal uses 3-level MLT-3 signaling employed by copper FDDI to reduce the signal frequen-

Table 1—Comparison of fast-Ethernet proposals

Specification	802.3U		802.12
Designation	100 BaseT		100 Base-VG 100 VGAnyLAN
MAC protocol	CSMA/CD		Demand priority
PHY (physical layer) designation	4T-Plus	100 Base-X	Quartet
Wire type	Category 3, 4, or 5	Category 5, optical fiber	Category 3, 4, or 5, optical fiber
Wire pairs	Four	Two	Four
Channel	Half-duplex	Full-duplex	Half-duplex
Block coding	8B/6T	4B/5B	5B/6B
Bit coding	NRZI	MLT-3 (ANSI XT39.5)	NRZI

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cy content on UTP cable. The scheme sacrifices the technical goal of less-than-30-MHz frequency content on the wires, however, by offering full-duplex transmission with only two wire pairs. The frequency content of 100 Base-X signals, therefore, mandates using data-grade (Category 5) UTP cable.

For new installations, using high-grade cabling is not a problem. Category 5 UTP cabling is now routinely installed in new network construction because its incremental cost is insignificant. Most networks, however, were built with voice-grade (Category 3) UTP cable.

To capitalize on that installed base, the 100 Base-VG proposal uses Category 3 cable in a scheme called quartet signaling. Quartet signaling divides the data stream among four wire pairs using 4B/5B block coding for error correction and NRZI bit coding for transmission. The result is half-duplex operation with each wire carrying a 30-MHz signal. If a better grade of wire or an optical fiber is available, the proposal allows the system to multiplex data streams together to take advantage of increased bandwidth.

Table 2—Fast Ethernet Alliance members

David Systems Inc
Digital Equipment Corp
Grand Junction Networks
Intel Corp
LAN Media
LANNET Data Communications Inc
National Semiconductor Corp
SEEQ Technology Inc
Standard Microsystems Corp
Sun Microsystems
SynOptics Communications Inc
3Com Corp

The IEEE 802 committee decided to have the 802.3U group augment the 100 Base-X proposal with a scheme that would utilize Category 3 UTP as well. That scheme, called 4T-Plus, uses four pairs of Category 3 wire with 8B/6T block coding. The data run on three of the four pairs; the fourth pair handles collision detection. Because of the coding scheme, the data wires handle a maximum frequency of 25 MHz.

The advent of a second physical-layer specification under 802.3U prompted the IEEE committee to designate 100 Base-T as an umbrella term for fast Ethernet with 100 Base-X and 4T-Plus

Switched hubs unclog system bottlenecks

The pace of standards development may be too slow for you if your Ethernet network is already approaching saturation. If only a few sections of your network need the higher speed, however, you have an alternative.

The IEEE 802 Committee's work focuses on providing 100-Mbit data rates to the desktop as part of a shared network. Switching hubs with 100-Mbit links (**Fig A**) can unclog your system under the right conditions. If your system uses the client/server architecture (**a**) or can be segmented into work groups with most of the traffic staying within the group (**b**), a switched hub can help.

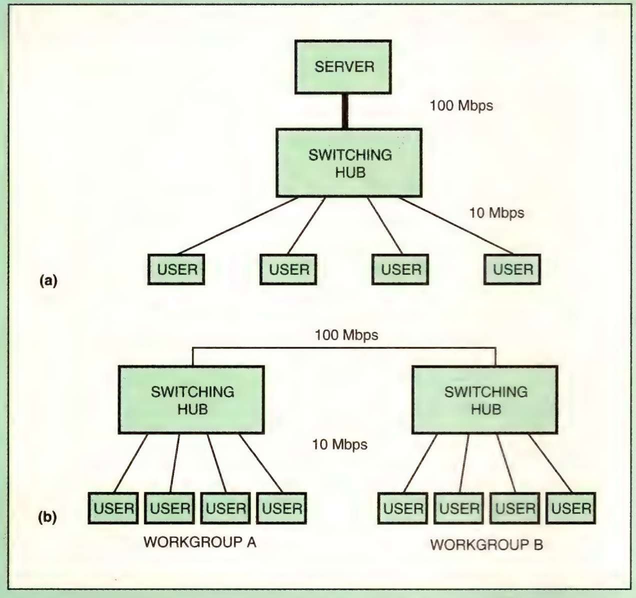

Fig A—Switching hubs with high-speed links can offer the equivalent of a dedicated network to individual users. They work best in client/server architectures (a) or in work groups (b) where traffic tends to localize within a group.

A switched hub dynamically establishes dedicated 10-Mbps Ethernet links between node pairs so that each user appears to have sole access to the network. The 100-Mbps link comes into play when the system needs to pass messages among hubs or to a server. FDDI can be used for the high-speed link, but fast Ethernet links don't require data repackaging and promise to be less expensive. Grand Junction Networks and Plaintree Systems currently offer switched hubs with 100-Mbit Ethernet links.

The Grand Junction hub, designated the FastSwitch 10/100 ($7250), offers 27 switched ports. A bridging port serves as connection to the corporate backbone, 24 are personal 10BaseT Ethernet ports, and two are fast-Ethernet ports. The hub's bridging port keeps local traffic off the backbone, reducing network congestion. The fast ports use the 100 Base-X signaling scheme, which Grand Junction originated, and can link hubs together or link the hub to a server.

The Plaintree hub, WaveSwitch, offers a mix of 10BaseT and high-speed ports. The 10BaseT ports can be dedicated to single users, connected to a shared Ethernet segment, or connected to another hub. The high-speed ports can use either FDDI for connection to a backbone or Plaintree's 100-Mbps WaveBus to connect hubs into a tree. The WaveBus link is Plaintree's proprietary version of a fast Ethernet. It uses the Ethernet data frame, but has the hub arbitrating network access rather than using CSMA/CD. The physical link uses two optical fibers operating at 850 nm.

WaveSwitch comes in two versions. The WaveSwitch 100 ($7250) includes 16 Ethernet ports and supports two additional high-speed ports. WaveSwitch 400 ($9125) handles as many as 112 Ethernet ports ($335) or 28 high-speed ports ($3350 for FDDI, $1200 for WaveBus) in a mix-and-match configuration.

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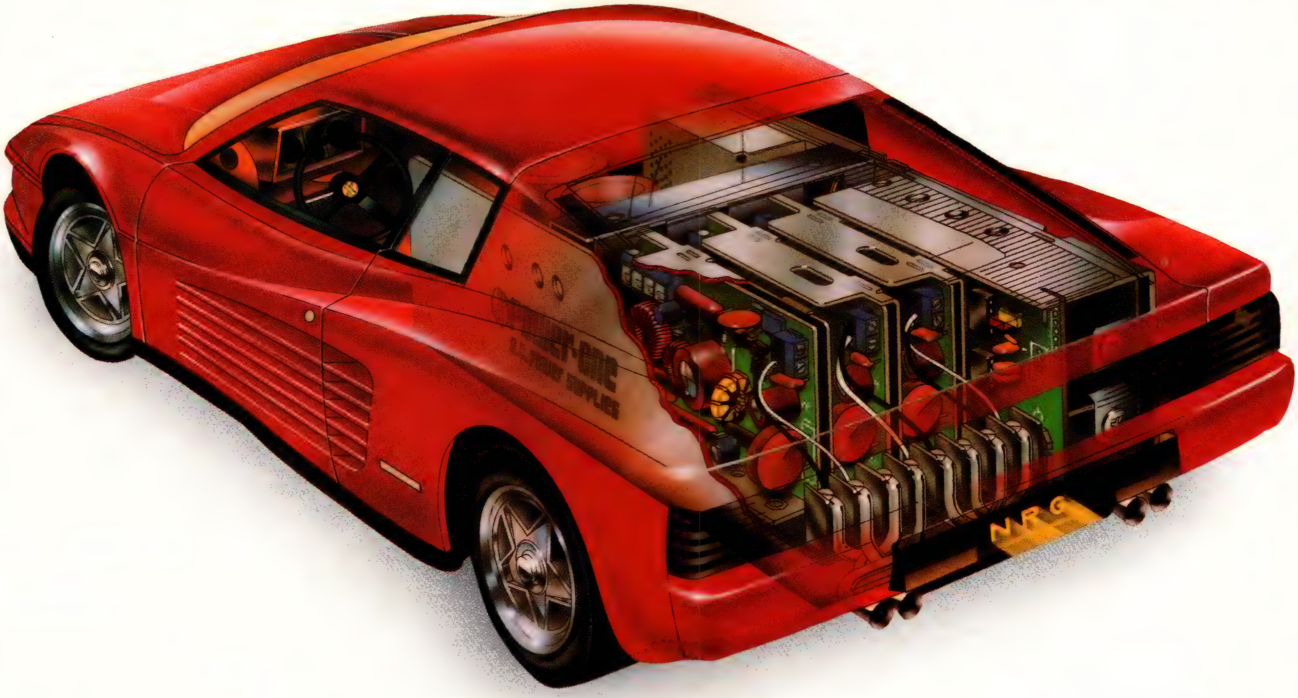

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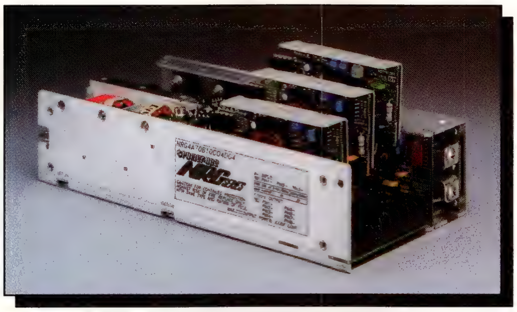

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Looking ahead

Until recently, debate over 100-Mbps Ethernet focused on which proposal, 100 Base-X or 100 Base-VG, would become *the* IEEE standard. The recent IEEE decision to pursue both has ended that debate; the conflict will now shift to the marketplace.

The reuse of carrier sense multiple access with collision detection (CSMA/CD) gives the 100 Base-X approach a considerable market advantage. All of the system software and silicon developed for Ethernet will transfer virtually intact to a 100-Mbps network—with only a frequency change. Unfortunately, all of the problems also transfer. The alternative approach, 100 Base-VG, represents a risk. It requires new and unproven software and hardware and may introduce problems of its own. Advantages include its deterministic access scheme and applicability to both Ethernet and Token-Ring networks.

In these lean economic times, expect reuse of existing resources as the approach favored by most of the market. The applications that require a deterministic access can be solved, at least in the near term, with switched hubs or carefully segmented network designs.

as subcategories for the two cabling types. The committee also elected to begin developing a media-independent interface for fast Ethernet similar to Ethernet's AUI (attachment-unit interface).

All of the fast-Ethernet proposals are still in committee, which implies at least a 6-month wait before the proposals attain draft-proposal status—and up to three years before they are full standards. In anticipation of the standards, products may begin to appear this year. AT&T and Hewlett-Packard have demonstrated working silicon of their quartet-signaling transceivers and anticipate releasing a complete 100 Base-VG chip set during the first quarter of this year. In addition, some nonstandard approaches have reached the market (see **box**, "Switched hubs unclog system bottlenecks").

Once both alternatives are represented in the marketplace, the success of either (or both) will ride on how well its (or their) developers predicted the market's response to MAC differences. Neither proposal provides an overwhelming technical advantage; hardware costs are likely to be comparable. The future of fast Ethernet boils down to a choice between speeding up what already exists and adopting a new protocol to guarantee timely access.

Technical Editor Richard Quinnell can be reached at (408) 685-8028, fax (408) 685-8028 and hit the star key.

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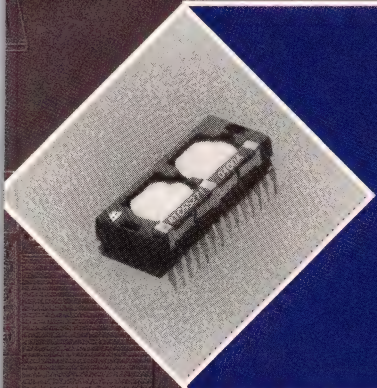

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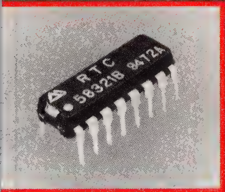

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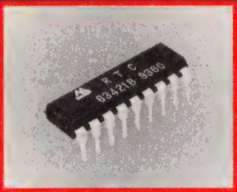

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- Alarm Function
- Access Time 120ns
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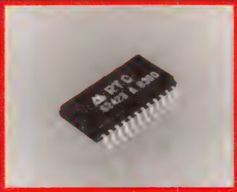

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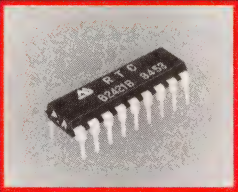

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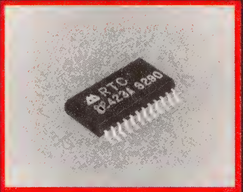

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- Second to Year and Day of the Week
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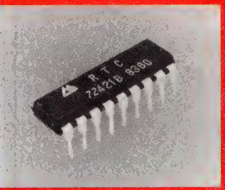

RTC 72421

- DIP 18 pin
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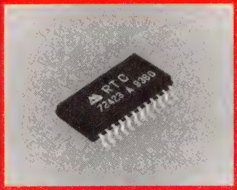
- Access Time 120ns
- Low Current Consumption



RTC 72423

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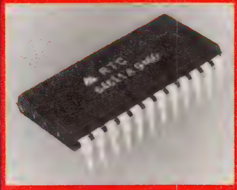
- Access Time 120ns
- Low Current Consumption



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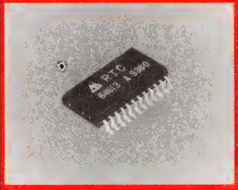

RTC 64613

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- Built-in Quartz Crystal
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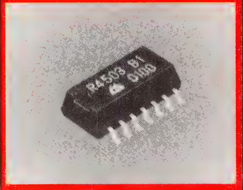
- Alarm Function
- Access Time 85ns
- 4bit Memory



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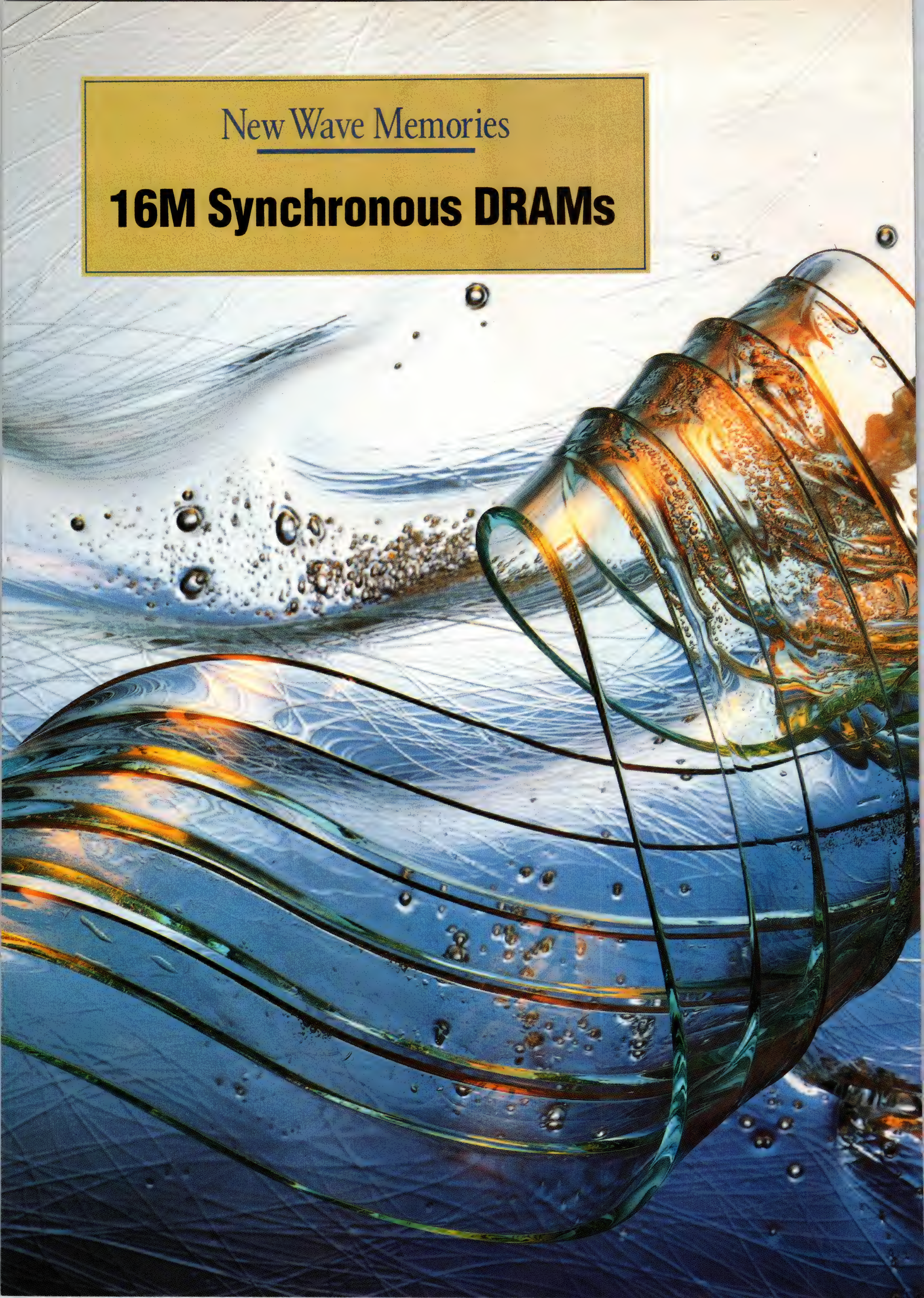

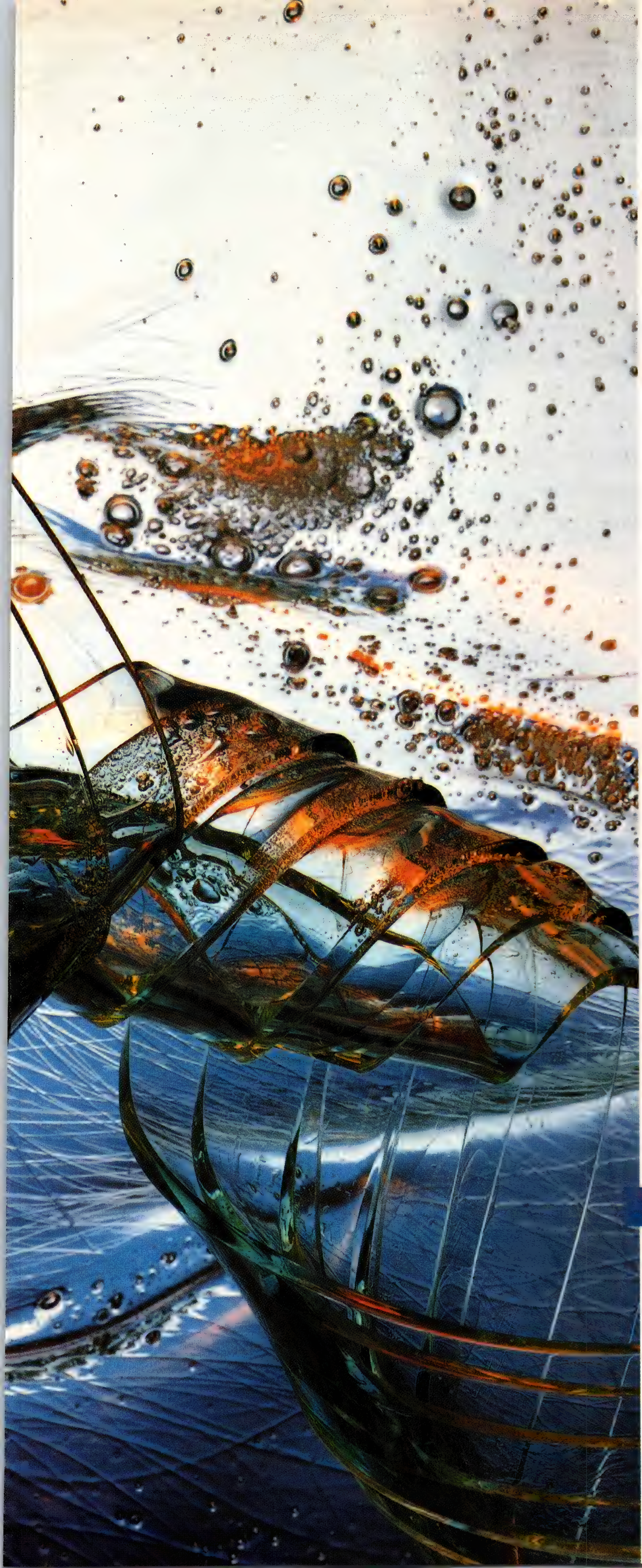

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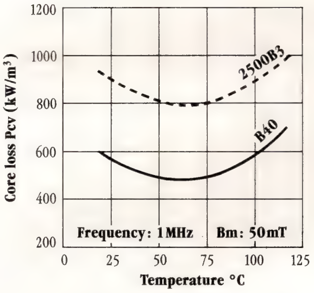
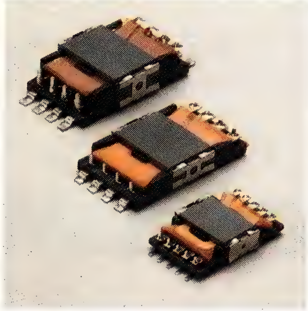
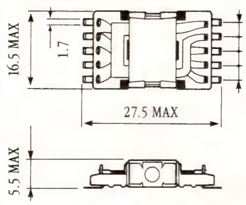
Curie temperature		Tc	(°C)	205	225
Density		d		4.8×10^3	4.9×10^3



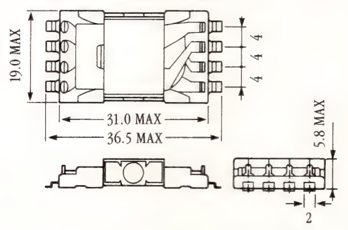


Shapes and Dimensions

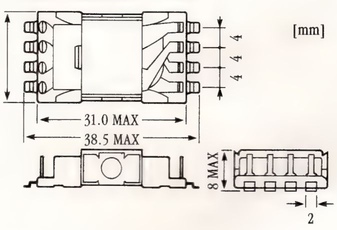
20-watt Transformer (FEE14)



40-watt Transformer (FEE18/5)



60-watt Transformer (FEE18/7)



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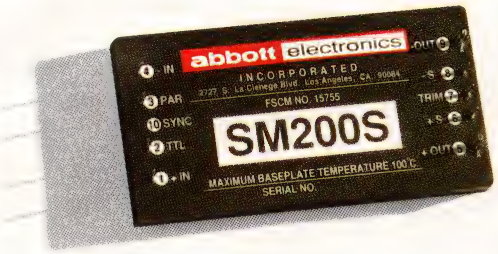
CIRCLE NO. 78



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- Board-mountable: *not*
- Readily available; not deliverable in unit form
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CIRCLE NO. 79

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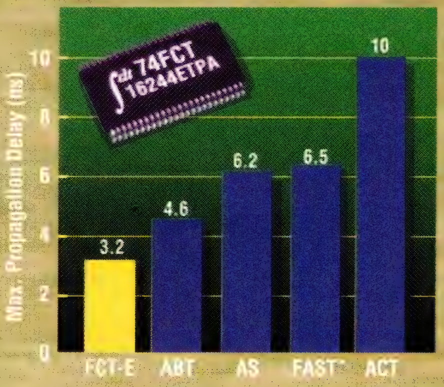

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FRONT-END WIRELESS PRODUCTS

Handheld-receiver front ends integrate assorted components

JOHN GALLANT, Technical Editor

Front-end products for handheld wireless receivers include amplifiers, spdt switches, antennas, attenuators, and filters. Unfortunately, most of these devices come as separate components, which the system manufacturer must wire together.

Cellular and cordless handsets place many demands on high-frequency semiconductors and antennas. Future PCS (personal-communication-service) communicators will push demands even further. Because these devices operate from batteries—which run at 5V currently, but certainly will run at 3V in the next generation—low current drain is critical for extending conversation time. In addition, handsets require a high degree of integration to keep designs compact. Thus, low cost is a must if the handset is going to be competitive in the commercial market. Antennas must be not only lightweight for portable applications but also durable and designed attractively.

Although a number of highly integrated chip sets accomplish baseband and modulation tasks for a variety of cellular and cordless handset standards (**Ref 1**), receiver front-end ICs are not as integrated. Designers must use a smattering of ICs that prepare the mobile antenna's RF signal before conversion to an IF signal. On the receiver side, a handset requires a low-noise amplifier (LNA), which interfaces with the antenna; a mixer follows to down-convert the RF signal to the IF signal. On the transmit side, the handset requires an up-converting mixer, which in turn drives a power amplifier (PA) to generate the RF transmit signal.

In addition, both the receive and transmit paths must connect to a single antenna in a manner ensuring that both paths do not interfere with each other. When the transmit and receive frequency are the same as

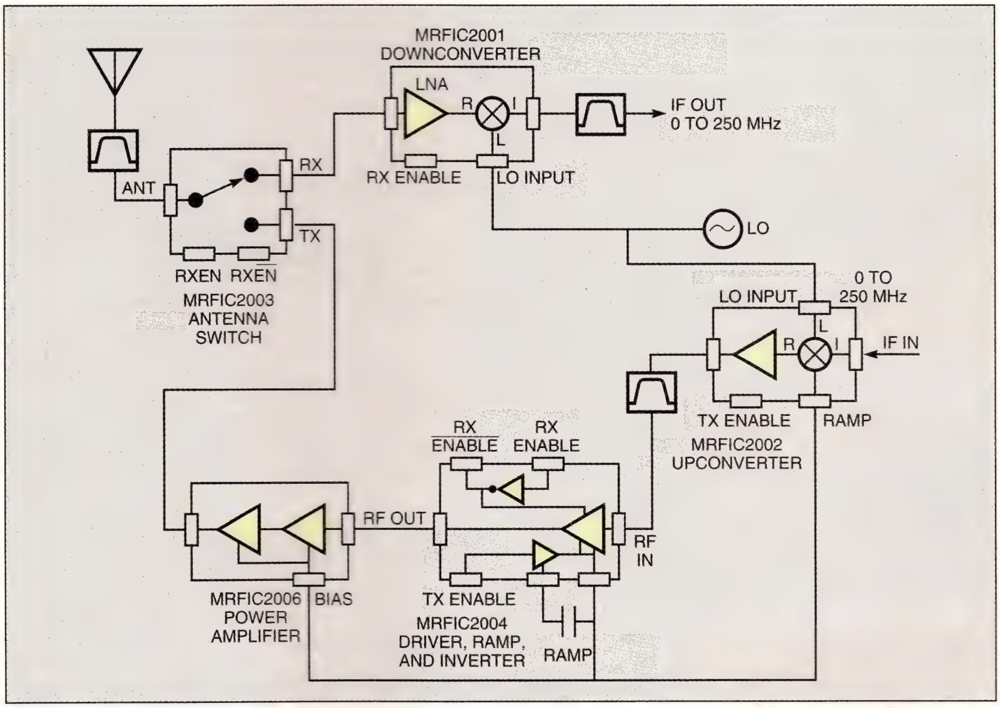
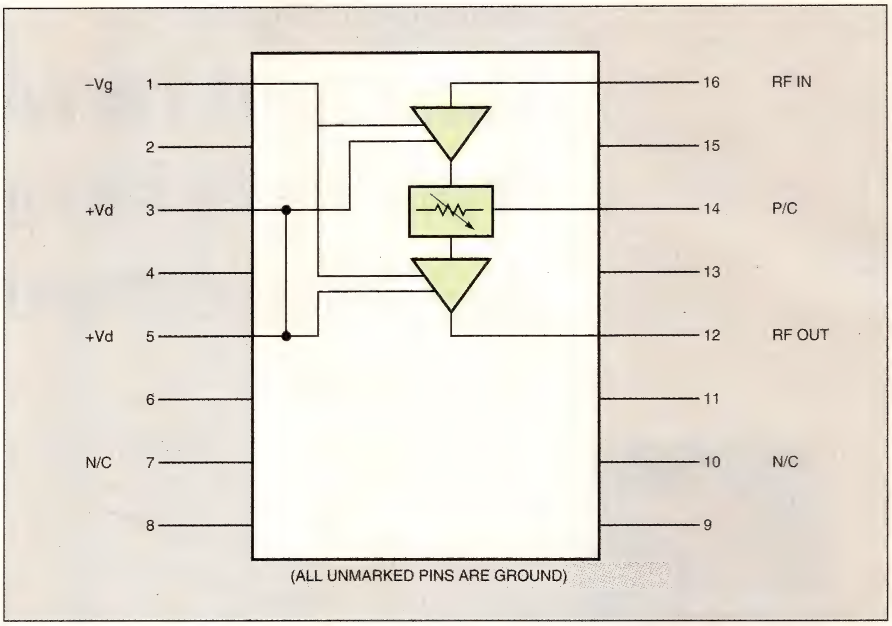


Fig 1—Motorola's 5-chip set for handheld, wireless 800- to 1000-MHz products shows the smattering of ICs necessary to implement a front end. Along with a handful of SAW filters, the chip set provides up and down conversion to a dc to 250-MHz IF.

time-division duplexing (TDD) (DECT and CT2 cordless standards use TDD), the standard antenna interface is a spdt switch called a transmit/ receive (T/R) switch. When the handset is receiving data, the switch connects the LNA to the antenna; when the handset is transmitting, the switch connects the PA to the antenna. The T/R switch should provide low insertion loss and enough isolation so that the transmit signal does not leak into the receive signal path.

When the transmit and receive frequencies are different as in frequency-division duplexing (FDD) (the IS-54 and GSM cellular standards use FDD), designers can connect the transmit and receive path to the antenna via a duplexer. A duplexer consists of two bandpass filters designed to pass only the receive frequency from the antenna to the LNA and to pass only the transmit frequency from the PA to the anten-

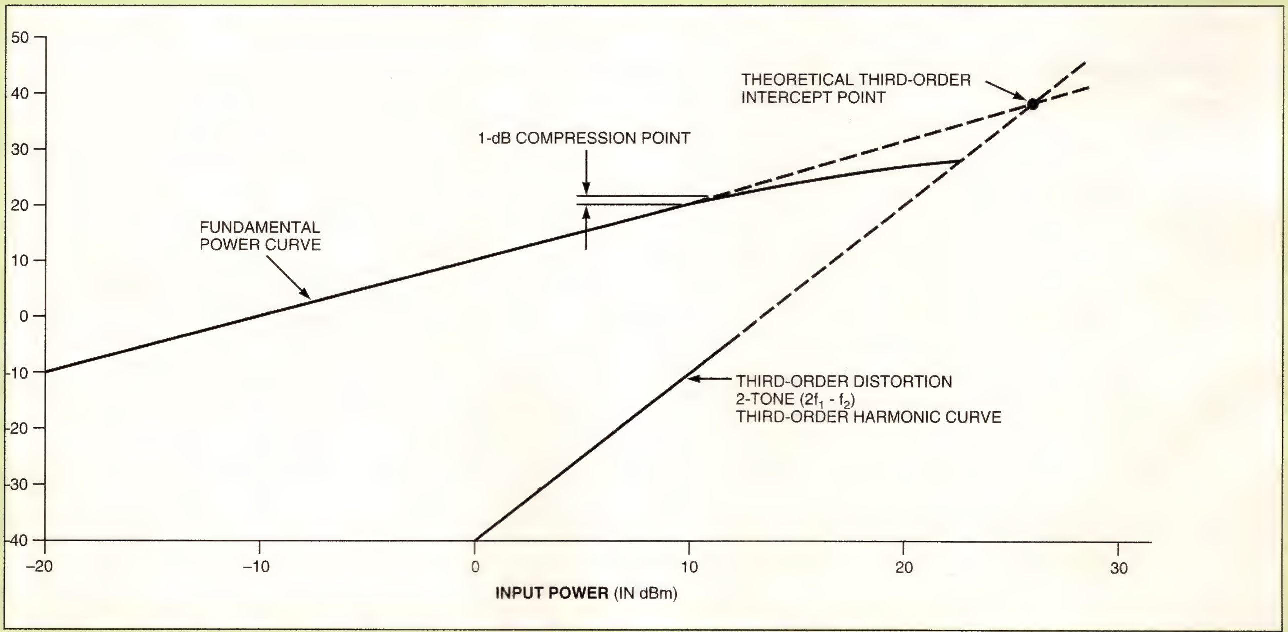


Model CMM1301 from Celeritek is a power amplifier for the 1.7- to 2-MHz PCS band. The amplifier provides 24 dBm of output signal and a power-control pin that can attenuate power over a 20-dB range.

A primer on handset specifications

If you are designing a handset and looking for typical receiver specifications such as maximum dynamic range, minimum signal-to-noise (S/N) ratio, or third-order intercept point in the standards for cellular, cordless, or ISM bands, you won't find them. These standards reflect FCC and ETSI concerns that one signal transmitting over the airwaves shouldn't interfere with another.

Thus, the standards specify a maximum saturated output power to which a mobile transmitter must adhere to prevent harmonics from causing interference. The standards also restrict the time-domain response of modulated waveforms to prevent modulation sidebands from spreading beyond their allotted bandwidth. As long as the handset designer adheres



The fundamental power curve of an amplifier theoretically intercepts with the third-order harmonic curve generated by two tones in the amplifier's baseband. The 1-dB compression point is where the amplifier just moves into saturation.

na. To improve isolation, some designs combine a T/R switch and a duplexer. Some wireless receivers use dual antennas to prevent signal loss due to a null in the antenna pattern. The dual antennas, which exhibit different antenna patterns, connect via another spdt switch, called a diversity switch.

Attenuators also play an important role in cellular-handset designs. Cellular base stations like to receive a relatively constant amplitude signal whether a transmitting phone is near or far. To accomplish this, the base station sends out a decrease-power command to a mobile phone that may be transmitting a strong signal as a result of its proximity to the base station. The mobile phone uses the command to control an attenuator in the transmit path, which reduces the received signal strength at the base station.

The RF and IF bandpass filters, which reject unwanted signals, are another major part of the handset. A bandpass filter placed at the RF antenna input passes only the specific frequencies for the cellular or cordless standard. A bandpass filter at the IF frequency rejects mixer harmonics and

Looking ahead

In the next six months, expect to see a variety of product releases for front-end components that cover 900-, 1800-, and 2400-MHz frequency bands. At 900 MHz, the offerings will be both silicon and GaAs, but at 1800 and 2400 MHz, the offerings will be almost solely GaAs. GaAs can attain higher gain and operates from lower voltages than can silicon. In addition, GaAs can attain a higher efficiency than can silicon at higher frequencies.

Efficiency is measured as the ratio of the third-order intercept point to the power consumed from the dc power supply. Typical GaAs efficiencies are 50 to 60%; silicon efficiencies are 20 to 30%. Motorola plans to offer a GaAs chip set for the 1.8- to 2-GHz frequency range in February. The company is also planning a 2.4-GHz GaAs product for release in 1994. In many cases, though, what is necessary is a higher degree of integration in front-end products to conform with the size constraints of handheld units.

to these restrictions, the design of the receiver/transmitter is left to the system equipment manufacturer.

Device manufacturers, however, should be aware of some of the equipment manufacturers' design considerations to deliver high-volume, low-cost, front-end parts. One consideration is the receiver's dynamic range, which is determined on one end by its minimum detectable signal (MDS) for weak received signals, and on the other end by its 1-dB compression point for strong received signals. A system's MDS is set by the receiver's thermal noise (−174 dBm in a 1-Hz bandwidth), noise bandwidth, S/N ratio, and receiver noise figure.

$$MDS=-174\ dBm+B_N+S/N+NF_R.$$

The receiver's noise figure is determined primarily by antenna gain, filter and switch losses, and the low-noise-amplifier (LNA) figure. To a first approximation, the receiver's antenna gain, which is approximately 2 dB, cancels the filter and switch losses (approximately −2 dB), so that the LNA noise figure is the defining factor for the receiver's overall noise figure. Considering some typical numbers for the MDS equation, the GSM specification for the channel spacing is 200 kHz, which approximates a GSM receiver's noise bandwidth. The 200-kHz bandwidth translates to 53 dB for the MDS equation. Allowing 20 dB for an adequate S/N ratio, the equation produces an MDS of:

$$MDS=-174+43+20+NF_{LNA}\ dBm$$
$$MDS=101+NF_{LNA}\ dBm.$$

If an LNA has a 2-dB NF, the MDS is −99 dBm.

The 1-dB compression point represents a point on the linear-input vs LNA-output-gain curve, which deviates from a straight line by 1 dB. The point determines where the amplifier just begins to enter its saturation region. Although the point is measured at the output of the amplifier, you can subtract the amplifier's gain in decibels to find the effective input 1-dB compression point. An amplifier with a −9-dBm-input, 1-dB compression point represents a dynamic range of 90 dB in our example.

System-equipment designers generally trade off an LNA's figure for a higher 1-dB compression point if all other specifications are equal. The reason is that the noise figure only affects the MDS, and subsequently only affects the place where a cell handoff occurs. The 1-dB compression point, however, represents the point where an amplifier begins to saturate, which should be as high as possible when a vehicle is close to a transmitting base station.

On the transmit side, the most important specification is the third-order intercept point of the power amplifier. The third-order intercept point is the theoretical intersection point of the fundamental power curve with the third-order distortion curve. Third-order distortion is caused by mixing two signals at the amplifier's input (**Fig A**). The third-order intercept point is a measure of the third-harmonic-distortion product the amplifier generates—and should be as high as possible. A rule of thumb for amplifiers is that the third-order intercept point is 10 to 15 dB higher in power than the amplifier's 1-dB compression point. Also, output-power specifications can be as high as 1W, so the transmit/receive switches must be able to handle high power levels.

image frequencies. These bandpass filters are usually SAW filters, which are small and lightweight and have virtually brick-wall passband-to-rejection band characteristics.

An example of the ICs you need to build a wireless-receiver front end is Motorola's MRFICxxxx 5-chip family of RF ICs for cellular and cordless frequencies (**Fig 1**). Along with some SAW filters, these silicon bipolar devices contain the front-end requirements to down-convert and up-convert an RF signal in the 800- to 1000-MHz frequency region to an IF signal that ranges from dc to 250 MHz.

The MRFIC2004 is an integrated driver and ramp circuit for the transmitters. The ramp is a burst-mode control integrator for TDD/TDMA systems, such as CT2 cordless phones. A power-

For free information...

For free information on the handheld wireless front-end products discussed in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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AT&T Microelectronics
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Celeritek
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Centurion International Inc
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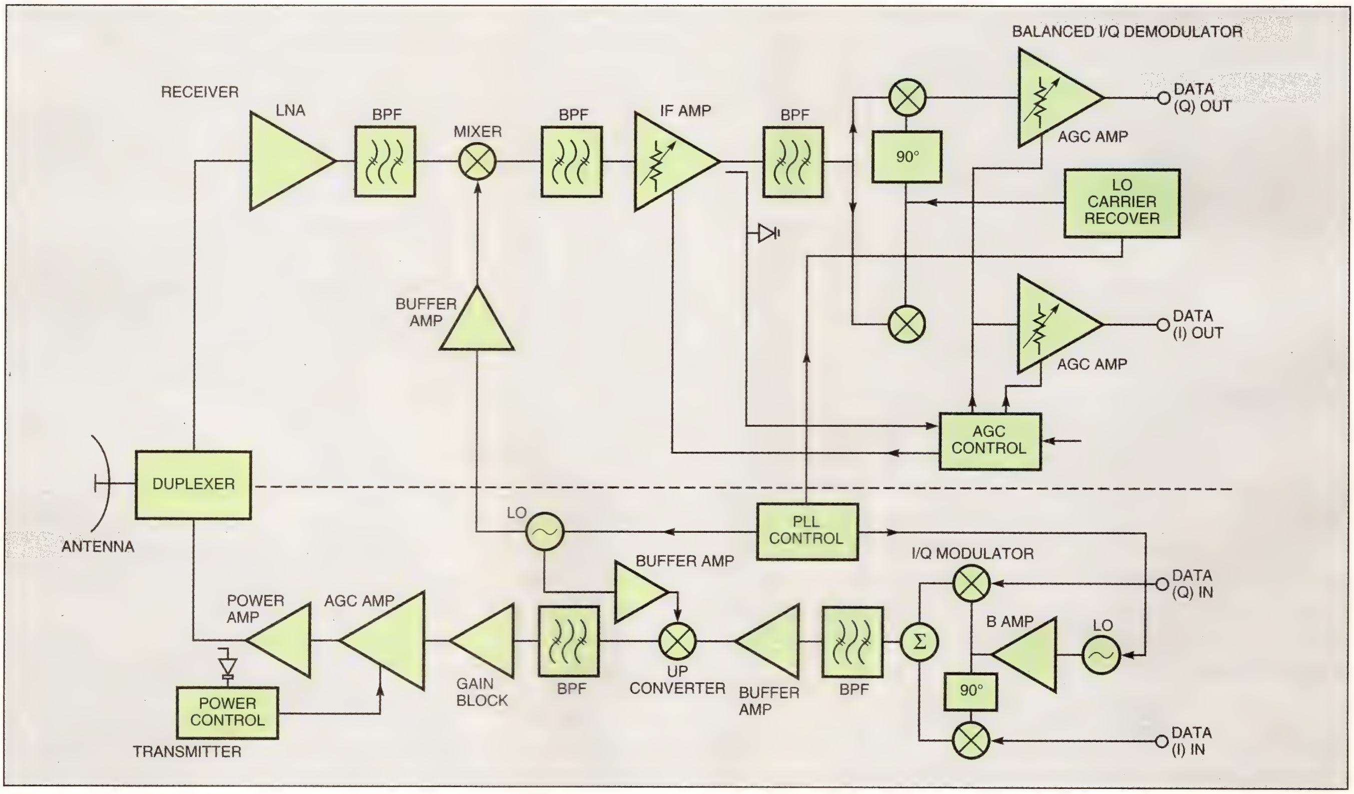

A block diagram of a typical digital/analog cellular, cordless, or PCS handset displays a variety of RF and IF components. M/A-COM supplies products for all of the shaded areas, albeit mostly as separate microwave monolithic integrated circuits.

down control circuit minimizes current drain. Also, an inverter provides complementary control for the MRFIC2003 antenna T/R switch. The MRFIC2006 provides power amplification; the MRFIC2001 handles down conversion. You can power down both devices when not in use.

A host of vendors offers LNAs, switches, attenuators, and power amplifiers for cellular, cordless, and emerging PCS markets (**Table 1**). Unfortunately, you probably won't find 1-stop shopping, so plan to search around to find all the ICs that match your system requirements. A receiver front end might comprise microwave discrete circuits (MDCs), microwave monolithic integrated circuits (MMICs), or microwave integrated circuits (MICs). MDCs consist of distinct circuits connected by transmission lines. MMICs consist of a semiconductor chip on which all active and passive components and their interconnections reside on the same substrate. An MIC is a combination of passive and active elements in hybrid form.

M/A-COM makes a variety of MMICs and antennas for the mobile wireless market. The MMICs include amplifiers, T/R and diversity switches, and attenuators. The company's catalog antennas cover 1.8- and 2.4-GHz bands for PCS and ISM, respectively. However, MA/-COM claims that most of its antenna designs are custom made. Its catalog parts have SMA connectors, which are primarily aimed at breadboard use only. One explanation is that Part 15 of the federal regulation for the ISM band prohibits using standard connectors in finished products. The company can alter the connector design or mount the antenna to a pc board per customer request. In addition, the company offers dual antennas that connect via a diversity switch.

Centurion International offers a variety of whip antennas for mobile wireless communications. The antennas fit a variety of mobile handheld units from GE, NEC, Panasonic, and Motorola. Typical half-wave dipoles are vertically polarized and feature a gain of 2.5 dBi. Antennas currently available cover a range of telecommunication frequencies. The antennas come in retractable-mount, molded-in suction-cup, fixed-right-angle, and adjustable 90°-angle designs; these antennas have a range of connector options.

Reference

1. Gallant, John, "ICs and modules for digital wireless telecommunications," *EDN*, August 19, 1993, pg 76.

Article Interest Quotient
(Circle One)
High 598 Medium 599 Low 600

Table 1—Representative wireless front-end products

Vendor	Part type/ model no.	Frequency band (MHz)	Gain (dB)/ power (mW)	Price	Features
Antenna Specialists Circle No. 420	CT-2 antennas/ ASP-873; ASP-870	860 to 870	3 (ASP-873); Unity (ASP-870)/NA	\$88 (ASP-873); \$85 (ASP-870)	Wall-mount design accepts unity or 3-dB gain antenna. Antennas have an omni pattern, a VSWR of 1.5:1, and N-female connectors.
AT&T Microelectronics Circle No. 421	RF amplifier/ 2121B	800 to 1000	11/2220 at 12V	\$33	Third-order intercept point=+42 dBm. Noise figure=3.5 dB. Operates from 12 or 15V dc. VSWR=1.2:1.
California Eastern Laboratories Circle No. 422	MMIC amplifier/ μPC2746T;	800 to 1000	18.5/ 22.5 at 3V	\$0.95 (OEM)	Noise figure=4.2 dB. Third-order intercept point=+6 dBm; silicon monolithic IC. Operates at 1.8V min.
	MMIC amplifier/ μPC2748T;	800 to 1000	19/18 at 3V	\$0.95 (OEM)	Noise figure=2.8 dB. Third-order intercept point=–1 dBm. Silicon monolithic IC. Operates from 1.8V dc min.
	MMIC amplifier/ μPC2745T	800 to 2400	12/22.5 at 3V	\$0.75 (OEM)	Noise figure=5.5 dB. Third-order intercept point=+8 dBm. Silicon monolithic IC. Operates from 1.8V dc min.
Celeritek Circle No. 423	Power amplifier/ CMM1301;	1700 to 2000 (PCS)	19/1000 at 4V (200 μW in standby)	\$13 (1000)	Power control over 20-dB range. 1-dB compresson point=+24 dBm.
	Power amplifier/ CAS1401;	1700 to 2400	18/1000 at 4V (200 μW in standby)	\$14 (1000)	Power control over 20-dB range. Integrated T/R switch. 1-dB compression point=+23 dBm.
	Power amplifier and LNA/ CAS1410	1880 to 1900 (DECT)	30/1100 at ±3V	\$16.50 (1000)	Power amplifier 1-dB compression point =+27 dBm. LNA gain=18 dB. LNA noise figure=2.2 dB. Integrated T/R switch.
Centurion International Inc Circle No. 424	Cellular antenna/ Model CXE	824 to 960	2.5/NA	\$11.75 (50)	Half-wavelength dipole design. 6 in. long and fits GE and Motorola cellular phones. Vertically polarized. VSWR=1.2:1.
Hewlett-Packard	MMIC LNA/ INA-03184	100 to 2500	25/40 at 4V	\$3.95 (100)	Noise figure=2.6 dB. Third-order intercept point=+7 dBm. Silicon bipolar device.

Table 1—Representative wireless front-end products *(Cont)*

Vendor	Part type/ model no.	Frequency band (MHz)	Gain (dB)/ power (mW)	Price	Features
Hewlett-Packard Circle No. 425	MMIC T/R Switch/ MGS-71008	DC to 3000	–1.2/NA	$9.85 (100)	GaAs-absorptive spdt switch. Switching time=3 nsec. Isolation=37 dB. Third-order intercept point=+45 dBm. VSWR=1.2:1.
	GaAs Power FET/ ATF-21186	500 to 6000	13.5 at 2 GHz/21 at 3V	$1.84 (100)	1-dB compression point=+19 dBm at 2 GHz. Noise figure=0.6 dB.
M/A-COM Circle No. 426	Dipole antenna / 3380-8030-0023	1850 to 1990 (PCS)	2.0/NA	<$10	Vertically polarized antenna for PCS. VSWR=2.0:1.
	MMIC amplifier/MAAM-41034	100 to 1600	15/105 at 3V	$1.95 (500)	Noise figure=5.5 dB. Third-order intercept point=+24 dBm. Silicon bipolar device.
	Diversity switch/ SW-923	DC to 2500	–0.7/0.1 at 8V	$13.50 (500)	Third-order intercept point=+65 dBm. VSWR=1.5:1. 1-dB compression point=+36 dBm.
	5-bit digital attenuator/ AT-260	DC to 2000	–1.9/NA	$14.30 (500)	31-dB attenuation in 1-dB steps. Attenuation accuracy=0.3 dB. Third-order intercept point=+39 dBm. 1-dB compression point=+27 dBm.
Mini-Circuits Circle No. 427	LNA/ VAM-6	DC to 2000	15/48 at 3V	$1.29 (25)	Noise figure=3.6 dB. 1-dB compression point=0 dBm.
	Power amplifier/ MAR-3	DC to 2000	12.5/175 at 5V	$1.70 (25)	Noise figure=6 dB. Third-order intercept point =+23 dBm. 1-dB compression point=8 dBm.
Mitsubishi Circle No. 428	Power amplifier/ MG7100 series	824 to 849; 872 to 905; 890 to 915	24.5/1200 at +6V		GaAs MMIC. 1-dB compression point =+31.5 dBm. 20-dB power control range. Operates from –55 to +150°C.
	Power amplifier/ MCF122	1850 to 1950 (PCS)	34/1000 at 5V	$40 (10)	GaAs MMIC operates from 3.4 or 5V. 1-dB compression point=+24 dBm. 20-dB power control range. Operates from –55 to +150°C.
Motorola Circle No. 429	LNA and mixer/ MRFIC2001	800 to 1000	23/14 (0.0005 in standby) at 3V	$2.33	Silicon bipolar device. 1-dB compression point=–10 dBm. Third-order intercept point= 0 dBm. Noise figure=5.5 dB. TTL-enable pin.
	T/R switch/ MRFIC-20003	100 to 1000	–0.8/0.65	$3.79	Silcon bipolar spdt switch. 1-dB compression point=+21 dBm. 23-dB isolation. Operates from 2.8 to 6.0V.
	Power amplifier/ MRFIC2006	800 to 1000	23/138 at 3V	$2.33	Silicon bipolar device. 1-dB compresion point=+15.5 dBm. Third-order intercept point=+25 dBm. Operates from 1.8 to 4.0V.
	LNA/ TQ9122N	100 to 2500	23/90 at 5V		Third-order intercept point=+6 dBm. Noise figure=1.3 dB. 1-dB compression point=–5 dBm.
Philips Semiconductors Circle No. 430	LNA, mixer, and VCO/ SA620	800 to 1200	12 dB (LNA); 8 dB (mixer) /26.4 at 3V	$5.22 (1000)	Integrates an LNA, mixer, and VCO on one chip. Noise figure=1.6 dB. Mixer input. Third-order intercept point=–2 dBm.
Phoenix Microwave Corp Circle No. 431	Power amplifier/ PA1007	800 to 900	14/1500 at 15V	$50 (OEM)	Noise figure=1.3 dB. Third-order intercept point=+33 dBm. TO-8 style casing. 1-dB compression point= +22.5 dBm.
RF Monolithics Circle No. 432	SAW filter/ PX1002	86.85	–2.7/NA	$25 (100)	IF filter for IS-54 digital applications. 3-dB bandwidth=±15 kHz. Ultimate rejection=65 dB. Intermodulation products for –20-dBm tones= –95 dBm.
Triquint Semiconductor Inc Circle No. 433	MMIC down-converter /TQ9201J	500 to 1600	20/47.5 at 5V	$5.75 (1000)	Noise figure=2.2 dB. Third-order intercept point =–9 dBm. Two selectable RF inputs allow for antenna diversity and gain control over a 30-dB range.
	MMIC LNA/	100 to 2500	27/ 90 at 5V	$4.60 (1000)	Noise figure=1.2 dB. Third-order intercept point =+3 dBm.
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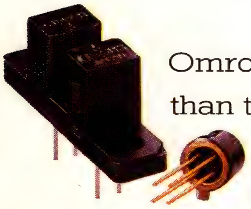

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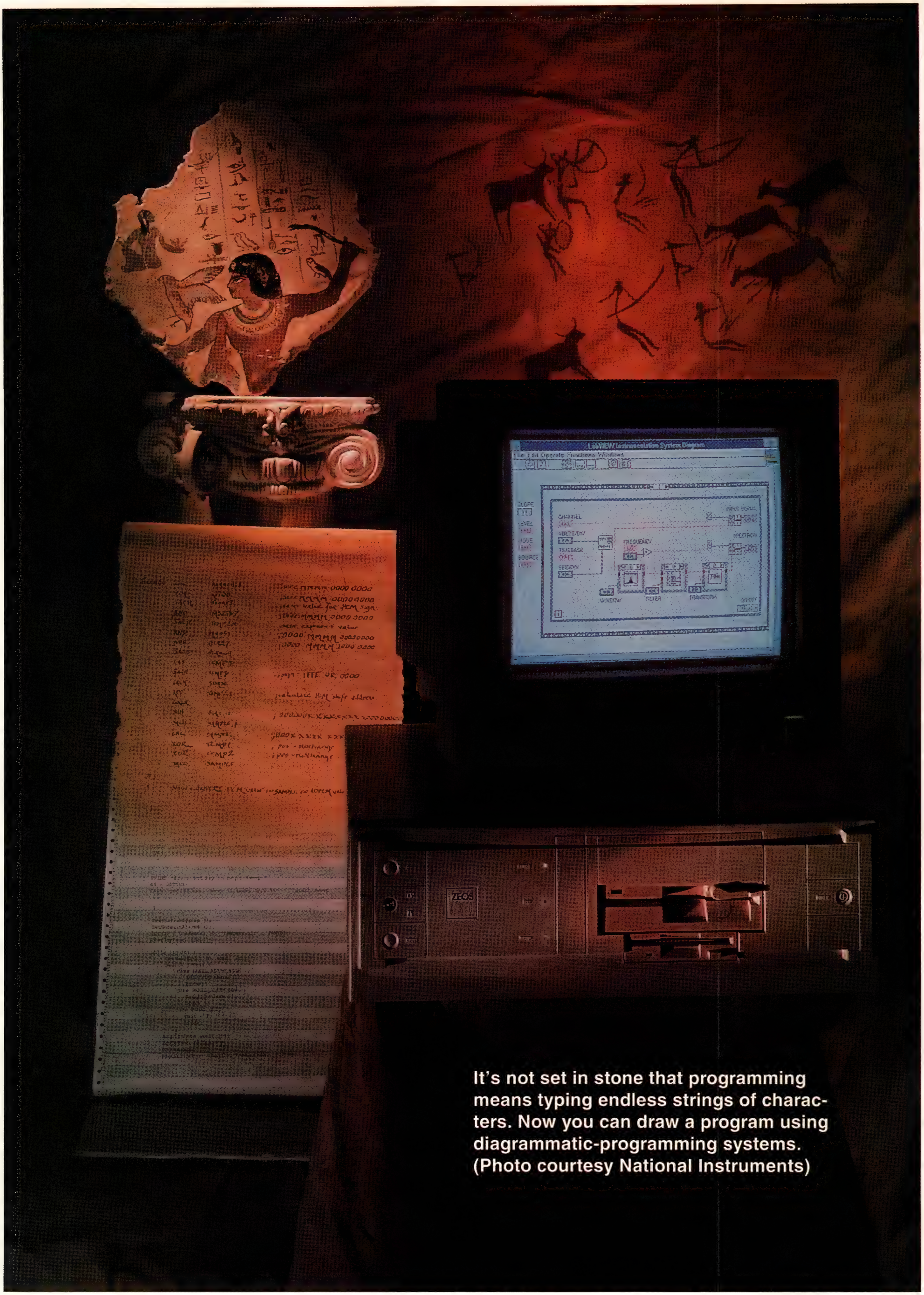
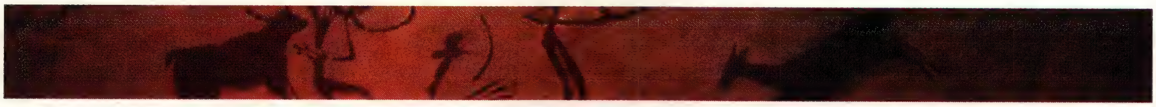


It's not set in stone that programming means typing endless strings of characters. Now you can draw a program using diagrammatic-programming systems. (Photo courtesy National Instruments)

EDN-SPECIAL REPORT

DIAGRAMMATIC



PROGRAMMING

CHARLES H SMALL, SENIOR TECHNICAL EDITOR

A host of diagrammatic-programming and debugging tools allows you to picture what your program is rather than making you describe in words what it does.

Programming used to mean just one thing: typing endless strings of ASCII characters into bottomless files. Luckily, you no longer have to extrude your software designs through the linear-sequential filter of text-based programming tools. Now you can work like an engineer, drawing a compilable diagram of what your design is rather than crafting a list of steps that it must perform.

The difference between textual programming and diagrammatic programming is the difference between a description and a mug shot, between a list of directions and a map, between a formula and a graph. In diagrammatic programming, the ideal is the real; the documentation is the program.

Diagrammatic-programming systems spring from elegant, clear ideas in the minds of their designers. These designers have taken the paradigms for their diagrammatic-programming systems from proven engineering practice, such as networked instruments; directed graphs ("bubble charts"); and DSP, circuit, and control-system diagrams. New diagrammatic compilers, based on diagrammatic software-analysis tools, are on the horizon.

Using diagrammatic programming, you can create what the computer-science mainstream has vainly sought for years: comprehensible software. Diagrammatic programming produces comprehensible software because diagrammatic programming taps the unsurpassed creative and analytical power of the visual hemisphere of the human brain.

Simply stated, while humans cannot even begin to approach computers' text-handling expertise, humans can still easily beat computers' pattern-recognition abilities.

Although programming-language designers pay lip service to *human* readability, the consumer they have in mind is clearly their compiler, not the poor programmers. All programming languages require humans to order their thoughts in a fashion easily ingested by computers. Therefore, programming languages introduce a high level of what Jeff Kodosky, inventor of National Instruments' LabView, terms "artificial complexity" into programming, making large programs literally incomprehensible to normal humans.

Diagrammatic programming can make easy what were once difficult software tasks. Writing, debugging, and verifying real-time software is, with the possible exception of DSP, probably the most difficult kind of software to write. But with diagrammatic programming, developing multitasking or multithreaded programs is effortless. You simply draw two lines of execution.

The technique of drawing programs is so new and its applications, so diverse, that the technique has no name. People label the technique "pictorial," "graphical," "iconic," or "diagrammatic" programming. Pointing up the lack of language skills in visually oriented people, some call the technique, oxymoronically, "visual language."

Although diagrammatic programming requires a good graphical user interface (GUI), don't confuse diagrammatic programming with a GUI itself or with software that merely creates GUIs, such as XVT's. Diagrammatic-programming systems are in the same league as programming languages.

Obviously, if you are going to draw a program, the computer you are working on must have high-resolution graphics. Indeed, the inspiration for many diagrammatic-programming systems was the Macintosh. Without a host computer such as the Mac, with its high-resolution graphics and graphics-oriented operating system, or a Unix computer running the X Window System, crafting a diagrammatic-programming system would be difficult. Because of its once-clunky graphics, the IBM PC was the last to acquire any diagrammatic-programming systems.

Diagrammatic programming is inherently better than text-based programming for two reasons: Humans, especially visually oriented engineers, can generate and comprehend pictures much more easily than they can linear lists of text. And, the linear structure of a text-based program simply does not match the structure of real programs. A multidimensional picture can model a complex program much more elegantly and succinctly than can any linear list.

Text-based programming languages, on the other hand, are a jumble of unrelated oddments. Programming languages confound constructs that loosely mirror mathematics with structures that mimic paperwork. Also thrown in the pot are commands derived from the innate testing and looping abilities of certain CPUs—C's increment operator, "++," being an egregious example. Tellingly, even the most modern software metaphor from the text-based world is no more than a messy pile of papers on a desk—windows, in other words.

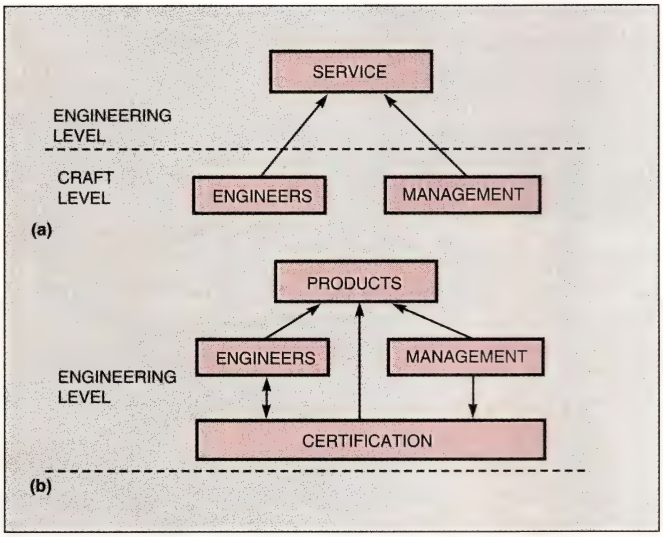


Fig 1—Text-based programming is not an engineering discipline (a), even if engineers are writing the software. Management contributes to the problem by continuing to view software as a service rather than as a product. In a schema for engineered software (b), engineers fashion software systems at the engineering level by designing and assembling software components. These engineers use diagrammatic programming systems, writing no code at all. Management directs the engineers to produce usable software components as products and sets up a certifying organization.

The computer-science mainstream periodically proclaims yet another variation on text-based programming that will magically transform programming from a craft into an engineering discipline. Remember "structured programming?" The latest such fad is "object-oriented" programming (OOP).

OOP takes as its model the hierarchy. (We can thank the Roman emperor Diocletian for the idea of hierarchy. He organized his empire into a rigid rank structure, which the Catholic Church adopted. Later, biologists employed the hierarchy concept in classifying plants and animals into a coherent scheme.)

Hierarchies have their limitations, however. As worthwhile as the biologists' ongoing task of classifying all plants and animals into a hierarchy is, such a scheme tells you nothing about *ecology*. That is, if you know the location of birds and worms in the hierarchy, you still don't know that birds eat worms for a living and not vice versa. Similarly, OOP does wonders for packaging like functions and deriving new offspring from their forebears. But the familial history of functions tells you little about how they interact when a program actually runs.

Because all these variations on text-based programming tools depend on human beings' feeble reading, writing, and text-comprehension abilities, the latest, hottest textual-programming method just never seems to pan out. And progress in hardware is making the situation worse: Advances in hardware engineering continue to outrace any advances in software engineering.

A common and very effective optimizing technique points up how incomprehensible large programs really are. All optimizing compilers perform "dead-code removal" as part of their bag of tricks. This optimization technique searches for and deletes all subroutines and functions that never get called. Compiler writers include this optimization technique because it is very simple for a computer to perform and because experience shows that all large programs are riddled with dead code like raisins in an oatmeal cookie.

Think for a minute, though: How does dead code come about? Clearly, at one point, a programmer took the time to craft a function or subroutine. That programmer would not have written that code for the fun of it. The programmer must have felt the code to be necessary. Yet other programmers working on the project who could have taken advantage of that code either forgot about it or never needed it.

If programmers used diagrammatic programming instead of textual programming, dead code would be as unlikely as civil engineers' drawing up blueprints for a road to nowhere. Comparing graphical tools that engineers use with programmers' development tools proves telling. Engineers' diagrams have two characteristics that set them apart. First, engineers' tools depend on powerful, formal systems of mathematics. Consider such graphical tools as Smith charts, Bode plots, pole-zero plots, and root-locus plots. Although these tools are intensely graphical, they suppress powerful mathematics.

The second distinguishing characteristic of engineers' graphical tools is that they allow easy bidirectional travel between the real and the ideal domains. Take a pole-zero plot, for example. Engineers can extract such a plot by analyzing a physical system. They can also tell much about a system by glancing at its pole-zero plot. But this process is eminently reversible. Engineers can dispose poles and zeros on a pole-zero plot in any fashion they choose to create an ideal system that has the performance characteristics they want. Then from this pole-zero plot, engineers can synthesize the specs for real components that, when assembled properly, yield a system that performs according to the idealized pole-zero plot.

From the ideal to the real and back

Conventional software tools do not exhibit these characteristics. The tools do not rest on powerful, formal mathematics, and they are not bidirectional. Until recently, you could only diagram a program. But to realize the program, you still had to concoct linear lists of unfathomable text. Now, with diagrammatic programming, you can actually *compile* your diagram. With the ability to compile software diagrams, the need to go back and forth from the ideal and real domains disappears.

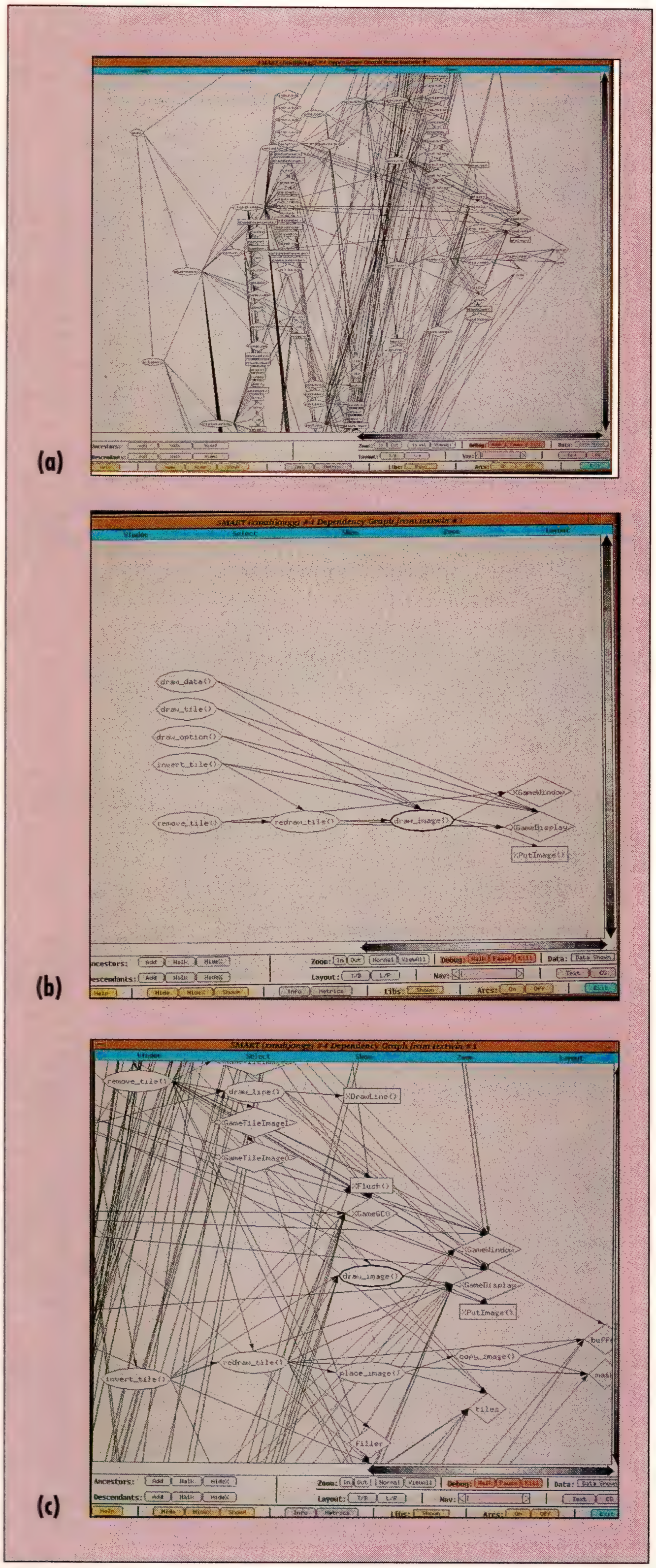
No text-based software-development system displays this level of bidirectionality or this kind of automatic optimization. In fact, in the programmers' lexicon, "optimization" means taking a stab at making a program as fast or as small as possible, not making the program achieve a complex, formally defined, performance specification.

Proponents of text-based systems can point to *relative* improvements in their craft with pride. However, in *absolute* terms, text-based programmers produce the most fault-ridden technological products available. Error rates in the percentages (of lines written) are the norm for large programs (**Refs 1** and **3**). Hardware projects of a similar level of complexity have error rates in the parts per million.

Advocates of text-based tools argue that new programs have high defect rates because all the components of the programs are crafted from scratch, whereas a complex new piece of hardware—an airplane, for example—is created out of existing components using established design methods.

Even if you grant the textually minded their view, just *why* does software development have to differ from other forms of technological development? According to proponents of text-based tools, the answer is that software is inherently much more flexible than hardware; hardware is very constrained, presumably giving hardware designers fewer wrong turns to take compared with the virtually infinite ways that software can go wrong. This observation merely raises another question: How did hardware come to be constrained in the first place? This constraint did not happen naturally to the hardware components as they ripened, hardening like nuts on a tree, nor will it happen naturally to software components. Indeed, the only evidence for software's peculiar properties is software itself.

Consider that for all new technological fields, except text-based programming, rapid progress at exponential rates followed an initial period of confusion. Examples are automobiles, aviation, and—of course—electronics. But in all the time that text-based programmers have been hacking away, they have not been able to accumulate the powerful mixture of art (practice) and science that practitioners in other tech-



Procase's Smartsystem can analyze a large undocumented C program, converting the program into a comprehensible bubble chart (a). The program has facilities for navigating through this directed graph of call dependencies and homing in on selected sections of the program being analyzed (b, c).

nological fields have. For example, reusable software components, such as Unix utilities and Fortran scientific subroutines that have been in use for more than 30 years, are still full of bugs.

Text-based programming once had its place

Engineers and programmers who have worked by themselves or on very small development teams might protest that they don't need any diagrammatic-programming systems. After all, high-quality, bug-free text-based software is possible. Lone programmers pursuing concrete goals, using languages and machines with which they are familiar, can do good jobs on small projects—if they have enough time and if their employers are willing to live with a 80:20% or worse software/hardware division of design effort.

The problem with text-based methods is that you cannot scale them up to large projects. An analogy would be building with mud bricks. You can build a perfectly satisfactory 2- or 3-story building from mud bricks if you site the building in an arid region. But don't build a mud-brick, 20-story hotel on a tropical seashore: It would wash away during the first heavy rainstorm if it didn't first collapse under its own weight. The technique just doesn't scale up.

Robert Troy, chairman and managing director of Verilog, agrees that something is wrong with the current state of software practice (**Fig 1a**). Writing software line by line is a craft comparable with building a wall brick by brick, says Troy. Further, text-based programming is not an engineering discipline, even if engineers are writing the software. But software practice is only half of the problem Troy sees. Engineers at least realize that writing software must become a form of engineering. Management contributes to the problem by continuing to view software as a service rather than as a product.

Fig 1b diagrams Troy's schema for engineered software. Here, engineers fashion software systems at the engineering level by designing and assembling software components. These engineers use diagrammatic-programming systems, writing absolutely no code at all. Management directs the engineers to produce usable software components as products. Management also sets up a crucially important new certifying organization that ensures that the software components are useful, functional, and bug free. Without the certifying organization, reusable software will continue to be just a dream.

Although Verilog already makes computer-aided software-engineering (CASE) tools for OOP and real-time systems, the company is working with Aerospatiale to develop general-purpose compilers that accept charts, graphs, and diagrams as inputs.

Conventional CASE tools do produce lots of charts, graphs, and specifications but no actual software beyond header files and function prototypes. Consequently, engineers who use conventional CASE tools labor mightily to produce a detailed design at the front end of a project. Then they go off for a year or two to code the design. Typically, at the end of the project, the resulting program bears no resemblance to the original design's documentation. As Troy sees it, the solution to this problem is to make the CASE material compilable.

The company will not field-test its diagrammatic compilers until mid-1994, and they will not be commercially available

Looking ahead

Text-based programming systems have a crucial weakness that renders them unfit for engineering: While a drawing can mimic, or symbolize, the actual structure of a device having parallel paths or feedback loops, a linear string of text is inherently a poor way to represent such structures. Anyone who has ever tried to write a real-time program can attest to how hard representing a complex control system in the form of a linear string of text is. "Hardware-description languages" are an even more gruesome method of representing these structures.

Then why have we been forced until recently to use text as a basis for a technological tool? Text-based tools are not designed with technologists' unique and powerful visual intelligences in mind. No, a passing familiarity with the arcane class of tools known as "compiler compilers" would reveal that the real consumer that these text-based tools are designed for is the compiler, not the technologist.

Those text-based-tool proponents who think that they need do no more than change some outdated "preferences" to gain acceptance of their products by technologists are trivializing a very fundamental and very important problem.

Creating technology takes extraordinary visual intelligence. Therefore, technologists' use of visual tools is not a mere "preference" any more than left-handedness or skin color is a preference. Engineers' visual tools have the form that they do because the tools have evolved over long periods of time to resonate with technologists' innate, genetically endowed type of intelligence. Remember, engineering predates not only programming but writing itself.

Writing, debugging, and verifying a text-based program is the devil's own curse. Very few humans have the ability and the inclination to putter with such a headache. With luck, these much more humane diagrammatic-programming tools will become prevalent, leaving text-based programming to those chosen few who have been gifted with the kind of intelligence that can handle such a chore. After all, we'll always need a few text-based programmers to write compilers.

Luckily, the availability of inexpensive but powerful PCs and workstations means that visual programming will become prevalent over the next few years. As a result, a terrific opportunity exists for visually oriented design tools that really suit the way technologists think and work.

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until late 1994. Verilog's software-analysis and reverse-engineering tool, Logiscope ($8000 to $15,000), provides a hint of what the company's version of diagrammatic programming might look like. Logiscope extracts graphs, histograms, and tables from a program to illuminate the program's structure, however large. The tool understands 90 programming languages and dialects, including Ada, C, C++, Fortran, and Pascal. It determines test coverage and recasts the structure of a program from one language to another. It runs under the Open Software Foundation's Motif specification.

A quick tour of some of the available diagrammatic-programming systems discloses that they fall into the following four broad categories—with some products overlapping categories:

- data-acquisition (instrument-con trol), analysis, and display software
- engineering simulators
- special-purpose program generators
- debugging tools

National Instruments began work on its diagrammatic-programming system, LabView ($1995), in 1984, qualifying the company as the undisputed pioneer of diagrammatic programming. When developing LabView, inventors Kodosky and James Truchard had a vision of "virtual instruments"—software entities that would plug together as easily as lab instruments do. Kodosky chose the data-flow diagram as a visual metaphor.

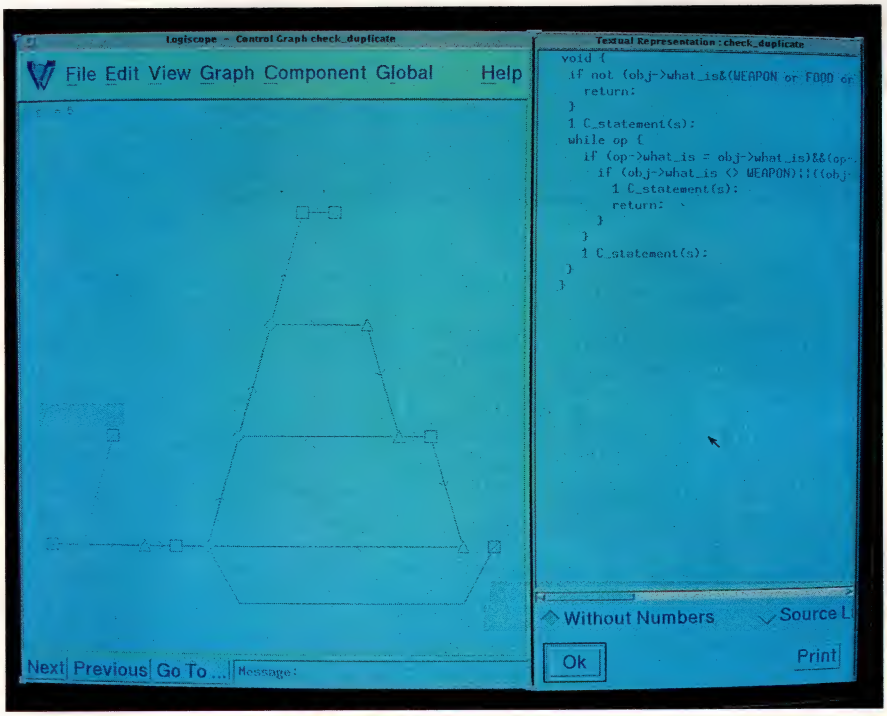
Conventional software diagrams, such as the data-flow diagram, invariably prove inadequate as compilable program descriptions. In National's case, the company's programmers had to immediately extend the data-flow diagram to make it into a complete program specification. For example, as soon as the first prototype was working, the need for icons that performed looping and iterating became painfully apparent. These icons perform the functions of common software constructs such as While, For, and Do loops. The company also concocted icons for control that correspond to CASE statements as well as an icon that impresses a sequential execution order upon segments of the data-flow diagram.

LabView's evolution is a story of continued improvement. It began life as an interpreted application program that ran only on Macs. But because National told LabView users that the product would allow them to simply draw programs, users expected the program to be as easy to work with as MacPaint. MacPaint cuts and pastes mere pixel fields; enhancing LabView to allow cutting and pasting program elements proved much harder to effect.

Next, LabView became a compiled application instead of an interpreted one to raise execution speed. Soon after, the need for a "runtime" version became apparent as users began to ship LabView systems as products rather than as services. The latest version of LabView is a true compiler, producing programs that run stand-alone. It also calls test routines written in other languages. The software now runs on Sun workstations and Windows PCs as well as Macs.

With LabView, as with other diagrammatic-programming systems, multitasking is effortless and crystal clear. If your application demands multitasking, you simply draw multiple streams of execution. Using textual programming for real-time programming results in murky code that rivals in incomprehensibility old-fashioned Fortran "spaghetti" code.

Note that National Instruments did not abandon text-based programming. The company finds that a certain percentage of test-program writers simply cannot use a diagrammatic-programming system. Lacking a foundation in cognitive psychology, National takes a stab at explaining this phenomenon by positing that some programmers are too used to text-based tools to be able to switch to diagrams. For these programmers, the company has a semiautomatic text-based program generator, called Lab Windows.

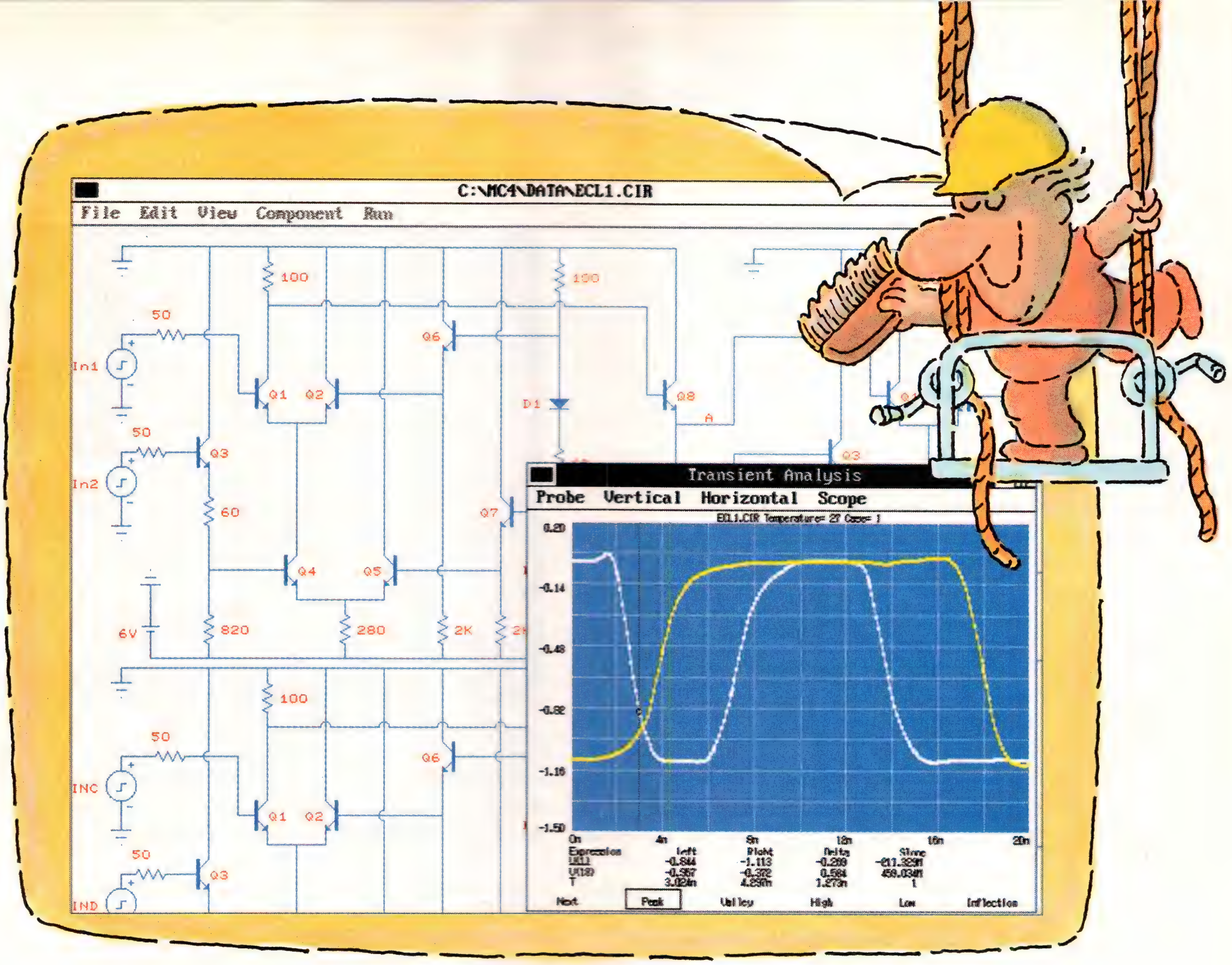


```
void {
 if not (obj->what_is&(WEAPON or FOOD or
   return:
 }
 1 C_statement(s):
 while op {
   if (op->what_is = obj->what_is)&&(op-
     if (obj->what_is <> WEAPON)||((obj-
       1 C_statement(s):
       return:
     }
   }
   1 C_statement(s):
 }
}
```

Pure Software's Quantify graphically displays software performance in a striking "river of time," pinpointing the routines that consume the most processing time.

Wavetek's WaveTest ($1995 for PCs, $6490 to $7995 for various Digital Equipment Corp computers) has evolved into a similar diagrammatic-programming system for IEEE-488, VXI, and RS-232C instruments. The latest version runs under Microsoft's Windows and supports dynamic data exchange (DDE). Wavetek combines two visual metaphors: The data-acquisition portion of the software employs the flow chart as a visual metaphor, and the analysis portion—a product developed by DEC—uses the data-flow diagram.

Wavetek had to add enhanced case, looping, and branching



Expression	Left	Right	Delta	Slope
V(1)	-0.844	-1.113	-0.269	-211.329M
V(18)	-0.957	-0.372	0.584	458.034M
T	3.024n	4.296n	1.273n	1

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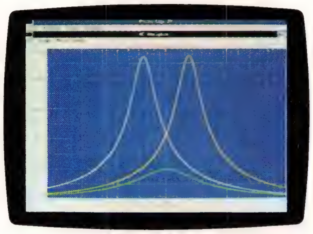

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icons to the standard flow-chart symbols. The company also added an interesting real-time construct to handle asynchronous service requests (SRQs) from IEEE-488 instruments. To set up a prioritized interrupt handler, you simply expand the SRQ icon and fill in a table. This table provides a clean and concise solution to what is a nasty bit of coding in other programming systems.

To accommodate text-based programmers, the company's VIP ($695) allows text-based programs to link to WaveTest's 200+ instrument-control drivers. The program includes a front-panel editor.

Also bridging data acquisition and display, as well as general-purpose simulation, is Hewlett-Packard's VEE (simulator, $995; IEEE-488 control, $5000). This software runs on HP 9000 computers under HP-UX (HP's Unix) and the X Window System. The visual metaphor for VEE (pronounced "vee") is the data-flow diagram. You draw your program by connecting icons. The software also comes with icons for engineering and mathematical operations. The icons themselves are examples of OOP and tend to be more complex and powerful than LabView's or WaveTest's. For example, the simple-seeming multiplication icon can perform any mathematically allowable multiplication. The icon can sense the types of the data that appear at its front end. The icon can multiply integers, floating-point numbers, complex numbers, and matrixes without specific instructions.

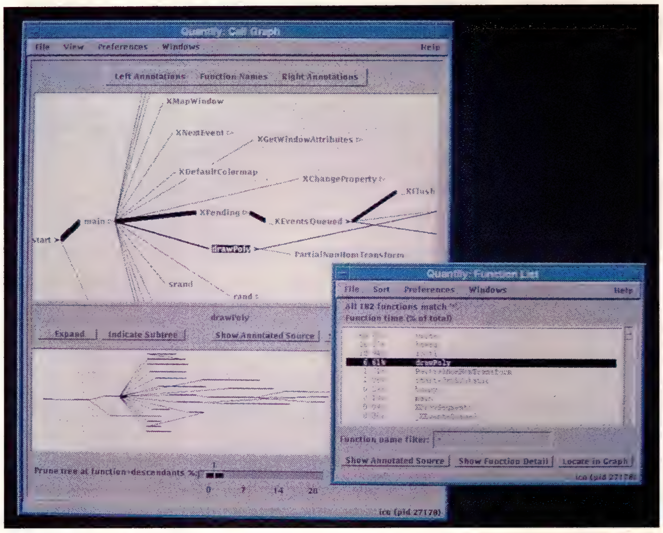
Not all test-software generators take a diagrammatic-programming tack. Capital Equipment's TestPoint ($995) takes an adamant anti-icon stance. This Microsoft Windows test-program generator reduces text-based OOP to the barest possible minimum. To concoct a test program, you drag and drop named objects from various collections into your "action list" (program). Some of the objects require you to type a few parameters. But you set up most objects in your action list for an application by selecting options from pop-up menus.

The software can multitask IEEE-488 and RS-232C instruments. One interesting feature is its ability to mix test results, schematics, and pictorial information. You can use this feature to make computerized equivalents of the famous Sam's "Photofact" annotated circuit diagrams. That is, you could aid test technicians by combining a circuit diagram showing a test point with a photo of a pc board. You could also display the required readings against the actual readings at that test point.

Keithley MetraByte's Visual-DAS ($99) takes a similar approach. The software allows a programmer to incorporate test routines for the company's data-acquisition boards into Microsoft Visual Basic for Windows programs simply by selecting and customizing objects. Meanwhile, Intelligent Instrumentation's Visual Designer adheres to the the diagrammatic-programming paradigm.

Software addresses specific tasks

Since DSP engineers have always manually diagrammed their designs, it's not surprising that several vendors have developed diagrammatic compilers for DSP. Without a diagrammatic compiler, DSP is a programmer's nightmare that combines arcane mathematical algorithms, abstruse physics, and quirky µP instruction sets into a horrific witch's brew.



Providing a hint of what one segment of diagrammatic programming might look like, Verilog's Logiscope produces a "control graph" representing the internal logical structure of a "software component." A node represents one or more statements or a decision point, and an edge symbolizes a control-flow transfer.

Comdisco's Signal Processing WorkSystem ($25,000), which runs on Unix workstations, began life as a simulator. The simulator accepted simulation programs drawn on workstation screens using engineers' DSP function blocks. Comdisco's visual metaphor is the engineers' familiar block diagram. Now that C compilers are available for DSP µPs, the system has evolved into a program generator as well.

Similarly, when Star Semiconductor developed its SPROC DSP chip, it also fielded its SPROClab diagrammatic-programming system ($5460). The IBM PC software allows you to interconnect standard function blocks to build signal-flow diagrams. It then compiles these diagrams directly over the DSP chip's hardware. (You can call these functions from programs written in other languages.) The software package also includes a debugger.

Other diagrammatic-programming tools for DSP come from Analog Devices, The Athena Group, Compass Design Automation (includes VHDL entry), Dynetics, Hyperception, Multiprocessor Toolsmiths, and Signal Technology.

However, diagrammatic programming isn't limited to test systems and DSP. Extend V2.0 ($695) from Imagine That Inc allows you to simulate complex systems on a Mac. This general-purpose dynamic-system simulator comes with function-block icons for amplifiers, filters, digital gates, and control functions as well as icons for mechanical systems and economics. The latest version has extensions ($990 each) for business-process reengineering and manufacturing. It also has data-analysis and display icons so that you can see the results of your simulation.

Integrated Systems' Matrix$_X$ ($2500 to $63,000) includes a diagrammatic-programming system exclusively for control engineers. The software, which runs on Unix workstations, accepts program specifications in the form of control engineers' block diagrams. Underlying the simple-seeming blocks are rigorous mathematical analytical engines for lin-

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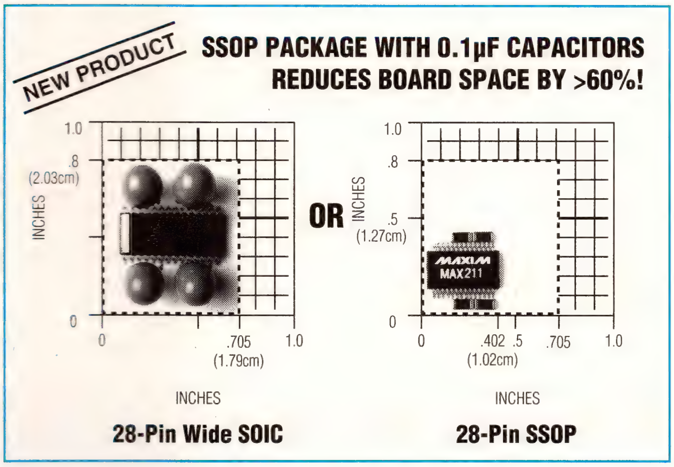

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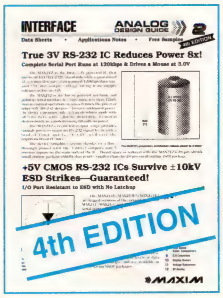
MAX561	4/5	1.0	✔	Complete +3.3V AT port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ear-system analysis. A fuzzy-logic system is also available.

The system first creates a non-real-time simulation from the block diagram. You can run this simulation from a virtual front panel, observing the simulation's response. The program displays outputs in graphical forms familiar to control engineers, such as Bode, root-locus, and Nichols plots. The software also incorporates measured data to simulate real-world devices and generates real-time source programs in C or Ada. The company also makes a Multibus-based simulator on which you can run programs in real time.

Another example of diagrammatic-programming systems are neural networks—the epitome of parallelism. For example, NeuralWare's NeuralWorks ($3995 to $7995) allows you to select any one of 28 major neural-network paradigms and dozens of variations. The software, which runs on PCs and common workstations, displays a diagram of the network you have chosen and lets you customize the network via a menu. As you train your network, the software displays diagrams of the network's evolving structure and outputs. Only when you are finished training your network does the software generate the C code that realizes your network.

A little-remarked-upon deficiency of text-based programming tools is that they suppress time. Not surprisingly, timing analyzers for digital circuits such as those from Chronology and Dr Design feature powerful graphical means for describing timing relationships.

If you've a hankering to try diagrammatic programming, you are not confined to grandiose, high-level projects such as designing an ASIC. Tao Research's GDS-11 ($1725) is a diagrammatic-programming system for the 68HC11 single-chip microprocessor that includes a compiler, a simulator, and a symbolic debugger. The software currently runs only on the Macintosh, but versions for Microsoft Windows and the 68HC16 are in the works.

Just like other diagrammatic-programming systems, GDS-11 makes multitasking effortless. You simply draw a state-transition diagram for each independent process. The state-transition diagrams act as visual metaphors and follow usual engineering practice with a few extensions. One minor change is that the states are in rectangular boxes instead of ovals because boxes are easier for a computer to draw than ovals. More important, you can subsume a collection of states and their relationships under a single state. That is, you can have submachines hierarchically ranked beneath a parent state

Manufacturers of diagrammatic-programming systems

For free information on diagrammatic-programming systems such as those described in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in EDN.

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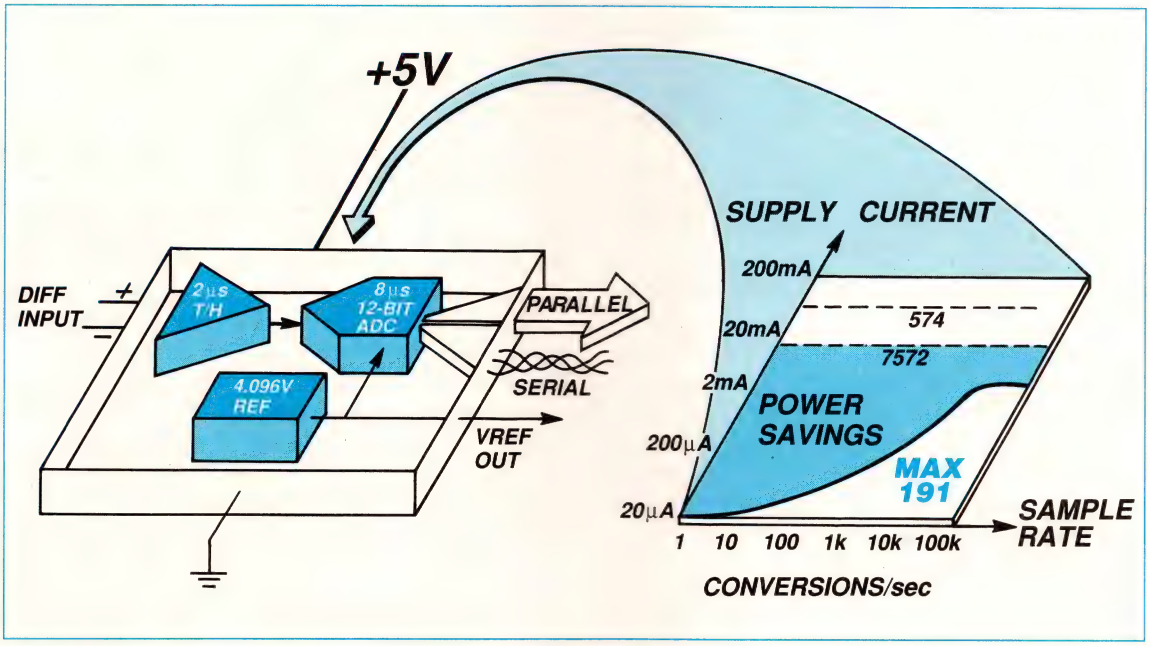

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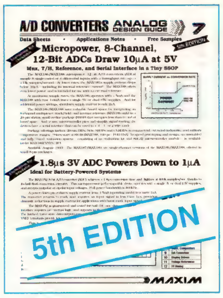

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machine. This facility proves handy when a state machine becomes too big or unwieldy to display on a Mac's screen.

As the capacities of gate arrays and field-programmable gate arrays grow, the need for special-purpose compilers that can handle such devices grows apace. One class of special-purpose digital-device compilers are "hardware-description languages" (HDLs). In a classic case of "give a carpenter a job to do and he'll think of a solution in terms of hammer and nails," textually oriented proponents of HDLs are bucking the trend toward making programming more like engineering; they want to turn digital engineering into programming. Instead of drawing a symbolic representation of what an electronic device is, HDL proponents would have digital engineers enter a text description of what it does.

The rationale for the switch from diagrammatic to textual methods is that gate-level symbolic systems are too cumbersome for large designs, necessitating a shift to a form of programming. And, of course, "programming" can only mean entering long strings of ASCII text into bottomless files.

Or does it? Consider architecture—a visually oriented profession if ever there was one. When architects design a house, they produce blueprints detailing every brick, every nail in every truss, every doorknob, and every hinge. But if architects are designing a large shopping center or planning a city, they don't abandon blueprints for text. They continue to produce visual designs but on a different scale and a different level of detail than when building a house.

Because HDLs must describe inherently parallel hardware elements with a sequential stream of ASCII characters, the "artificial complexity" of HDLs is even higher than that of conventional programming languages. So complex are HDLs that even experienced users caution against using more than a tiny, proven subset of an HDL's full range of expressiveness.

Further, even ardent HDL advocates admit that HDLs do a poor job of handling random logic. HDLs fare best on regular hardware structures, providing an easy way to size such structures for specific applications by changing a few parameters. But stripped of the artificial complexity of a text-based programming language, such scalable HDL constructs reduce to a fill-in-the-blanks chart—a staple of diagrammatic-programming systems.

One vendor, i-Logix Inc, has pursued a diagrammatic path to "synthesizing" digital designs. The company chose a prodigiously enhanced state-transition diagram as one of its visual metaphors. The company's booklet (**Ref 2**) describing the enhancements is worth reading to improve your manually drawn state-transition diagrams. Along with the enhanced state-transition charts, the software provides an activity chart for diagramming process views, functions, activities, interfaces, and data flow. Last, a module chart shows how the components of the architecture relate physically.

The company's first product, Statemate V5.0 ($20,000 to $40,000), simulates finite-state machines on Unix workstations. You draw a state-transition diagram and other supporting documentation on a workstation screen. You then link your state machine to a simulated operator's control panel, and "operate" your state machine. Recent improvements allow you to use a finite-state-machine chart as a template with which you can instantiate multiple examples of that chart. The software now also aids you in correlating system requirements with the state machines you have designed. Such "requirements traceability" is easy because it lets you directly compile engineering documents rather than using an HDL. Similarly, Ractive Concepts' Betterstate ($995) turns enhanced state charts into C code.

Another product from i-Logix, Express VHDL V3.0 ($32,500), turns your state machine into an HDL listing in VHSIC HDL (VHDL). You can then compile the resulting VHDL listing into an ASIC. In other words, you can realize an elegant finite-state machine in an ASIC at the press of a key without writing any code.

Charting a slightly different course, Redwood Design Automation's Reveal ($65,000) takes VHDL and Verilog HDL text files as inputs. The software then abstracts the HDL elements in compact, visual representations. You can manipulate the structure of these representations as well as simulate the diagrammed systems.

Diagrammatic tools can also help you make sense of text-based source code. For example, Procase's Smartsystem ($35,000) can convert an ugly, undocumented, 1-million-line C program into a comprehensible directed graph (bubble chart). The software has facilities for navigating through this directed graph of call dependencies and homing in on selected sections of the program being analyzed. It also automatically finds dead code and a variety of syntax errors.

Another debugging tool, Pure Software's Quantify ($1198), analyzes a program to determine "watchpoints." Thus, it comprehensively analyzes the execution of an entire program, including calls to shared and third-party libraries. Setting a flag during Make operations enables the performance measuring; it requires no recompilations or special libraries. The software, which runs on Sun workstations, graphically displays the gathered performance information in a striking "river of time," pinpointing the routines that consume the most processing time.

Finally, Wind River Systems' WindView ($4995) graphs with 1-μsec resolution the dynamic behavior of multitasking software systems. The software presents a time line of the actual sequence of high-level system activities, such as task switching, interrupts, semaphore operations, and message passing. EDN

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3. Wiener, Lauren Ruth, *Why We Should Not Depend on Software*, Addison-Wesley, Reading, MA, 1993.

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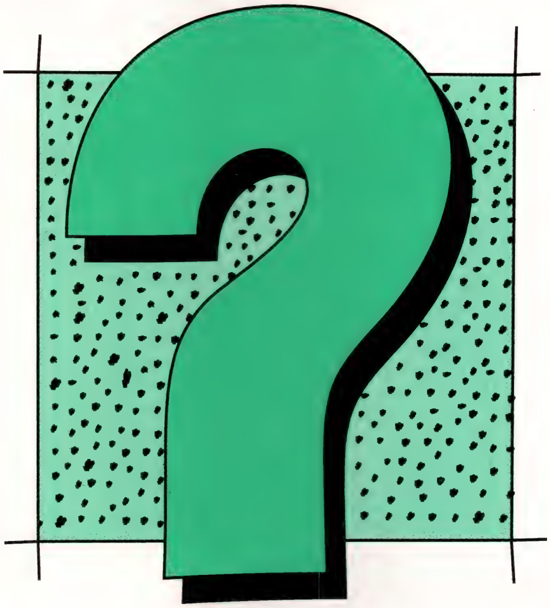

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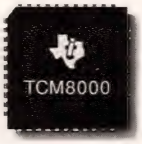

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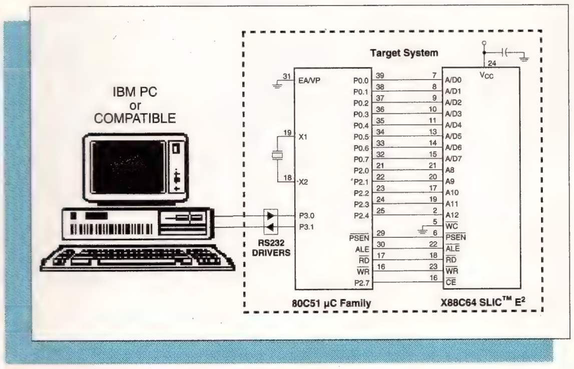
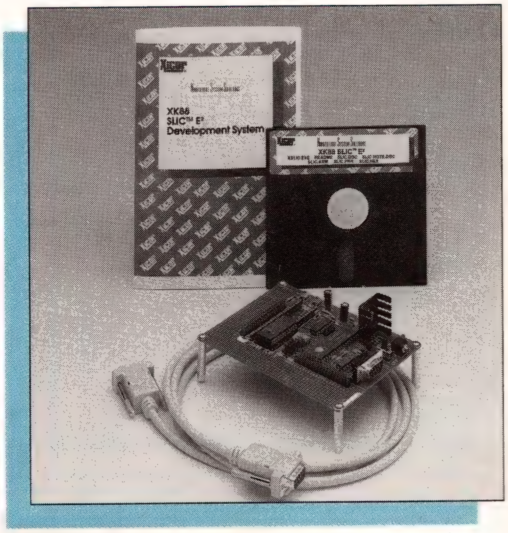


System example using an 80C31 and an X88C64 SLIC.

Data Sheet Enclosed

XK88 / 80C31 SLIC™ E² Development System



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The XK88 is available from Xicor or Xicor's distributors. To order a XK88 SLIC E² Development System directly from Xicor.

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CIRCLE NO. 91

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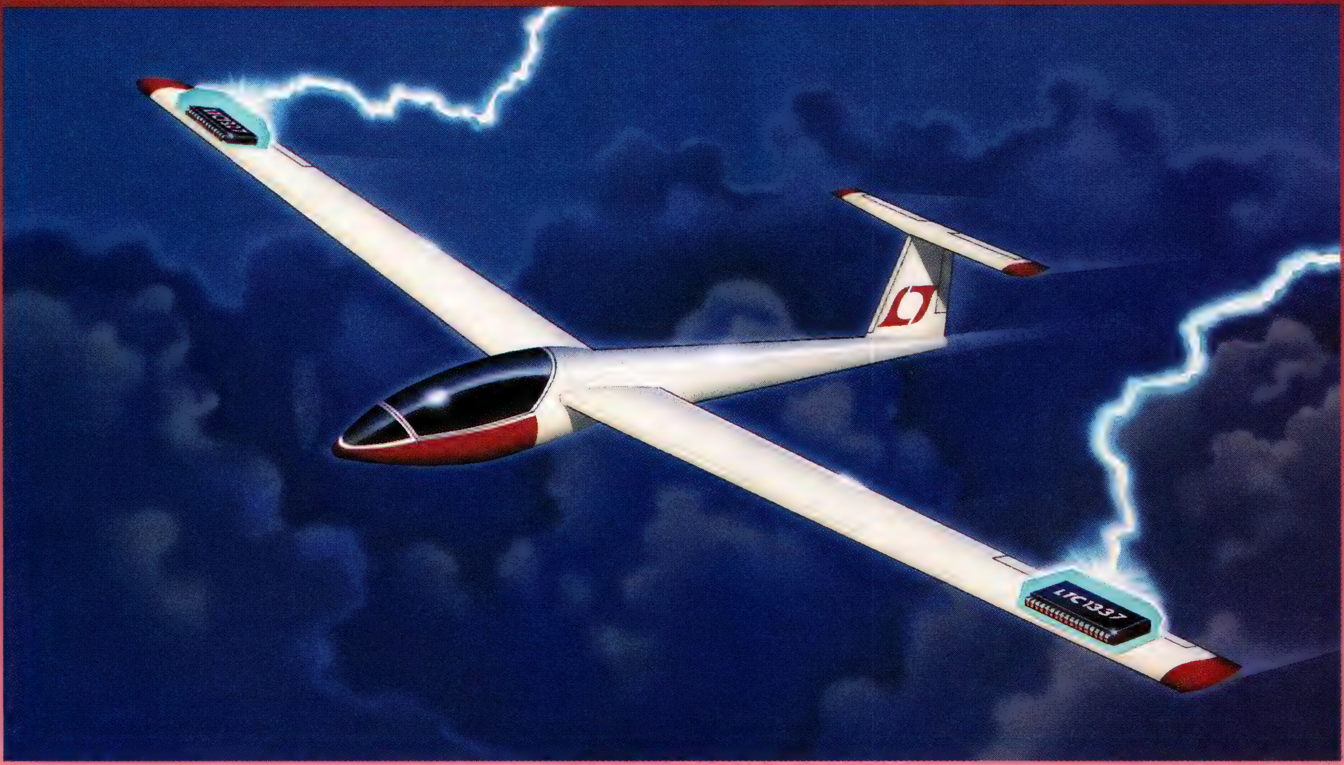

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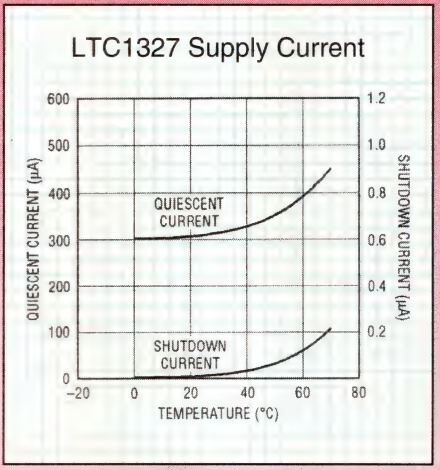

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CIRCLE NO. 92

EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

Modulator's design cuts FPGA's gate count

Bernie New, Xilinx, San Jose, CA

The pulse-width modulator (PWM) macro in **Fig 1** requires only half as much logic as a conventional 2-counter design. With the help of extra logic, a synchronous, loadable up/down counter can encode information in the duty cycle of a constant-frequency, constant-amplitude signal.

In **Fig 1**, a flip-flop toggles whenever the counter reaches its terminal state, causing the counter to alternately count up and then down from its preloaded value. If you load the counter with a value P, then the length of the down-count period is P+1 clock periods, and the length of the up-count period is 2^n–P clock periods. The toggle period of the flip-flop is the sum of these two periods, 2^n+1 clock periods. This period is independent of the preloaded value P.

Consequently, the flip-flop's output is the desired PWM signal. The period is constant, and its high time is proportional to P+1. Xilinx application note "Simple Loadable Up/Down Counter," XAPP 002, details the counter. EDN
EDN BBS /DI_SIG #1350

To Vote For This Design, Circle No. 469

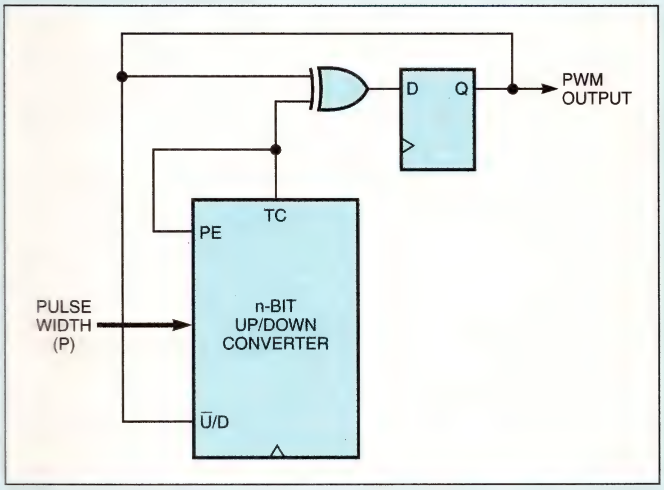

Fig 1—With the help of extra logic, a synchronous, loadable up/down counter can perform pulse-width modulation in an FPGA. This modulator requires only half as much logic as a conventional 2-counter design.

Line driver economically synthesizes impedance

Victor Koren, Orckit Communication Ltd, Ramat-Gan, Israel

The line-driver circuit in **Fig 1** uses a second op amp to synthesize the output impedance. The conventional line-driver circuit employs a single op amp having a resistor whose resistance is equal to the desired impedance in series with the op amp's output. The principal drawback of the conventional circuit is that the single op amp must deliver twice the needed output voltage because of the large voltage drop across the output resistor.

The circuit in **Fig 1** is similar to the famous Howland current pump but has different resistor values. To calculate the output resistance, R_O, short the input to ground. Then

$$V_{OZ}\times R_1/(R_1+R_2)=V_O\times R_1/(R_1+R_3),$$

where V_{OZ} is the output voltage with the input shorted.

$$\begin{gathered}V_{OZ}=V_O\times(R_1+R_2)/(R_1+R_3)\\ I_{R5}=(V_O-V_{OZ})/R_5=(V_O/R_5)\times\\ (1\text{-}(R_1+R_2)/(R_1+R_3))=(V_O/R_5)\times(R_3-R_2)/(R_1+R_3)\\ R_O=V_O/I_{R5}=R_S\times(R_1+R_3/(R_3-R_2)\end{gathered}\qquad\textbf{(1).}$$

After fixing the values of R_1, R_2, and R_S, to calculate R_3 for a given R_O, use

$$(R_3 3R_4+R_O 3R_2)/(R_O-R_5).$$

You can dispense with unity-gain buffer IC_2 by connecting R_3 directly to the output. The line driver's output impedance in this case is the value that **Eq 1** gives in parallel with the series connection of the resistors R_1 and R_3.

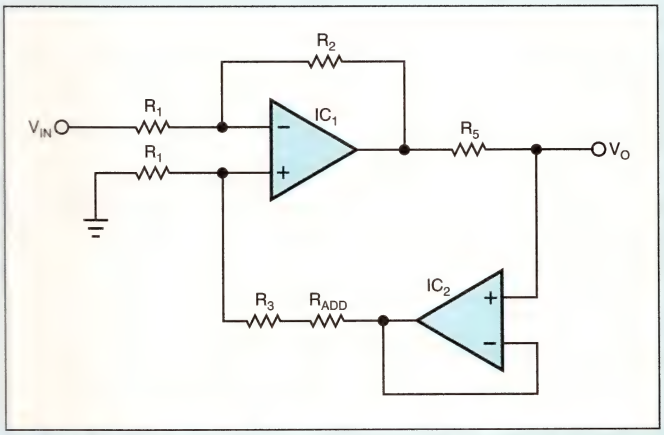

Fig 1—This line-driver circuit uses a second op amp to synthesize the desired output impedance rather than inserting a power-hungry resistor in series with the op amp's output.

For this scheme to work, all resistors must have very close, matching tolerances. One way to ensure close tolerances and, at the same time, reduce cost is to use thin- or thick-film networks for R_1, R_2, and R_3. However, for the circuit to work, R_3 and R_S must match closely. So you will have to add a precision resistor, R_{ADD}, in series with R_3 to bring their total resistance exactly up to R_S's. **EDN BBS /DI_SIG #1351** EDN

To Vote For This Design, Circle No. 470

Converter has high efficiency at low loads

Dana W Davis, Maxim Integrated Products, San Jose, CA

The high overhead of most dc/dc converters' normal supply currents do not permit high efficiency at low load currents. The micropower components and circuit design of the converter in **Fig 1**, however, enable it to maintain 90% efficiency for load currents below 8 mA.

For example, the quad Schmitt-trigger NAND gate, IC$_1$, draws a maximum quiescent current of 0.25 µA, and the combination voltage reference and comparator, IC$_2$, draws about 2.5 µA.

The circuit's boost regulator, comprising Q$_1$ and associated components, uses pulse-width modulation (PWM), and the circuit supplies gate drive to switch Q$_1$ only when needed. Further Q$_1$ is a low-$R_{DS\text{-}ON}$ device, minimizing I^2R losses in inductor L$_1$.

The comparator IC$_2$ turns the PWM boost regulator on and off. When the boost regulator is off, the entire circuit draws about 6 µA. IC$_2$ compares its own reference voltage against the circuit's output, V_{OUT}. The resulting comparator output (pin 8) is high when V_{OUT} is above its threshold and low otherwise.

The NAND gates form a combination oscillator, flip-flop, and buffer inverter. The flip-flop blocks oscillator pulses to the gate of Q$_1$ when the comparator's output is high. When the comparator's output goes low, the pulses pass through to the gate of Q$_1$, activating the boost regulator.

R$_1$ and R$_2$ help determine the circuit's dc output level:

$$V_{OUT}=V_{REF}(1+R_1/R_2).$$

The output voltage ripple for light loads depends on the comparator's hysteresis. With R_3=2.4 MΩ, the hysteresis in millivolts equals the value of R$_4$ in kilohms. Then, the ripple in millivolts equals

$$V_{RIPPLE}=V_{REF}(1+R_1/R_2)(R_4),$$

where R$_4$ is in kilohms. For the circuit in **Fig 1**,

$$V_{RIPPLE}=1.182V(1+18/1.5)(1)=15.4\text{ mV}.$$

EDN BBS /DI_SIG #1349

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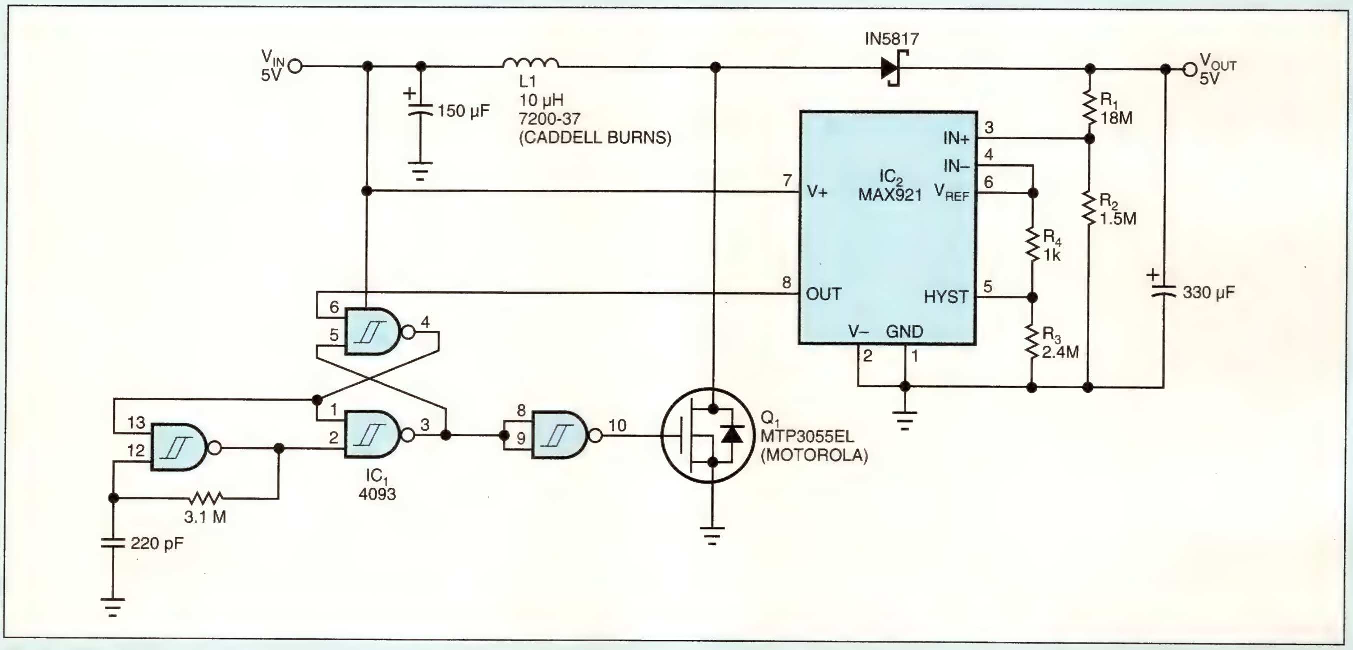

Fig 1—The micropower components and circuit design of this converter enable it to maintain 90% efficiency for load currents below 8 mA.

Classic detector enables low-cost receiver

Charles Kitchen, Analog Devices Inc, Wilmington, MA

Using modern discrete JFETs and ICs, you can build a low-cost super-regenerative receiver that has µV-level sensitivity at VHF and above. Such receivers also boast very low parts counts and low power consumption. Super-regenerative detectors are practical for wideband FM reception as well as for AM. They even can somewhat detect high-amplitude, narrowband, FM signals.

The circuit's sensitivity is better than 1 µV, and it oper-

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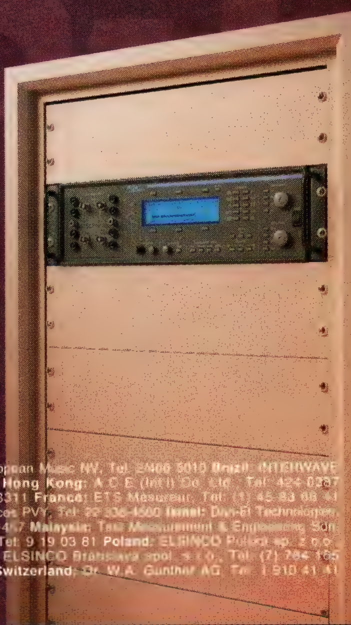

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CIRCLE NO. 93

ates over a wide range of VHF (**Fig 1**). You can build this small receiver for about $20. It draws less than 10 mA from its two 9V batteries.

The circuit comprises an RF stage, a super-regenerative detector, and an audio amplifier. The RF stage, Q_1 and associated components, prevents the receiver from radiating its own signal back out the antenna and helps to eliminate dead spots in the receiver's tuning range. These dead spots arise from antenna-resonance effects.

The capacitively coupled output of the RF stage connects to a tap on coil L_1. You have to determine the tap's exact location by experimenting; the higher up the tap is on the coil, the greater the sensitivity, but also the greater the loading on the detector.

The super-regenerative detector, Q_2, is essentially a modulated oscillator whose input is coupled to the antenna via the RF-isolation stage. This section alternates between oscillating and being periodically quenched.

The periodic quenching resets the oscillator, allowing the input signal to build up again to very high levels. Small noise sources require greater periods of time to build to a self-sustaining free oscillation than do higher amplitude radio signals. Therefore, given the limited time between quench intervals, the signal sources get amplified to a much greater extent before they are quenched out than do any noise sources. Note that the oscillations must fully decay before being allowed to start up again. Even a small amount of residual signal initiates a premature free oscillation—ending all useful amplification for that period.

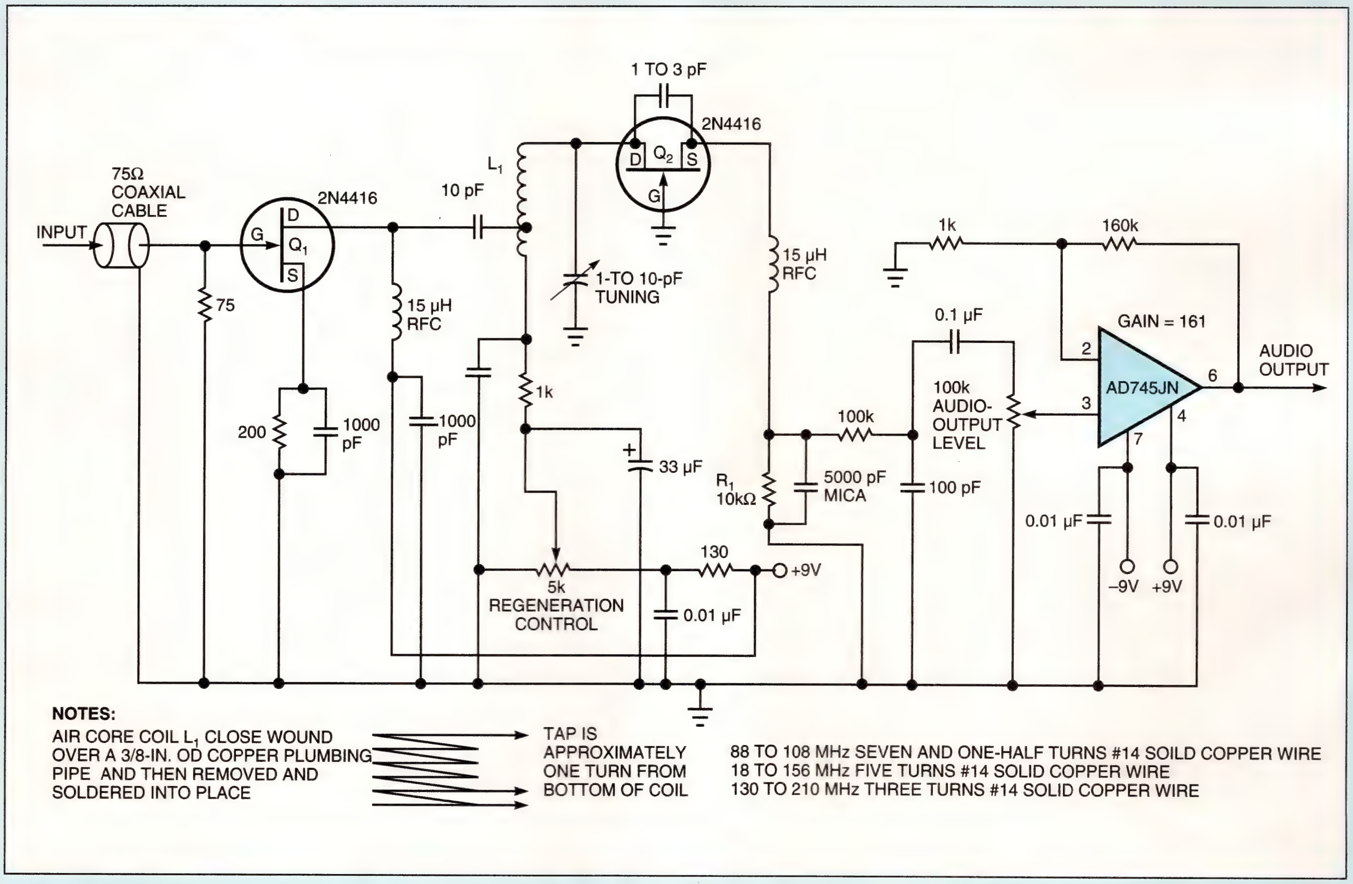
In this circuit, the RC time constant of R_1 and C_1 is long enough that capacitor C_1 cannot discharge fast enough (at the signal frequency rate) through R_1. This lack of discharging builds up a variable dc voltage across R_1 and C_1. This voltage periodically quenches the main oscillator. The 5-kΩ regeneration control sets the detector's operational voltage and also functions as the quench-frequency adjustment.

A 2-pF capacitor provides RF feedback between the FET's source and drain, causing it to oscillate. You may need to increase or decrease this capacitor's value by 1 pF or so to compensate for variations in your circuit's layout. A 15-μH RF choke keeps the FET's source above ground at RF.

The output of the detector drives a low-noise, op-amp, output stage. A simple lowpass filter removes the quench voltage from the detector's audio output.

Because super-regenerative detectors handle VHF, stray circuit capacitances or multiple ground paths can prevent the detector from oscillating. You absolutely must locate the super regenerative detector's tuning coil away from other objects—particularly chassis ground, the bottom and sides of the equipment enclosure (if it is metal), and any shielding.
EDN BBS /DI_SIG #1348

To Vote For This Design, Circle No. 472


1 TO 3 pF
2N4416
D
Q2
S
G
L1
75Ω COAXIAL CABLE
INPUT
2N4416
G
D
Q1
S
10 pF
1-TO 10-pF TUNING
15 μH RFC
75
15 μH RFC
1k
200
1000 pF
1000 pF
33 μF
+
R1 10kΩ
5000 pF MICA
100k
0.1 μF
100k AUDIO-OUTPUT LEVEL
100 pF
1k
160k
GAIN = 161
AD745JN
2
3
6
7
4
AUDIO OUTPUT
0.01 μF
0.01 μF
−9V
+9V
130
+9V
5k REGENERATION CONTROL
0.01 μF
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TAP IS APPROXIMATELY ONE TURN FROM BOTTOM OF COIL
88 TO 108 MHz SEVEN AND ONE-HALF TURNS #14 SOILD COPPER WIRE
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Fig 1—This super-regenerative receiver's sensitivity is better than 1 μV, and it operates over a wide range of VHF. It draws less than 10 mA and costs about $20 to build.

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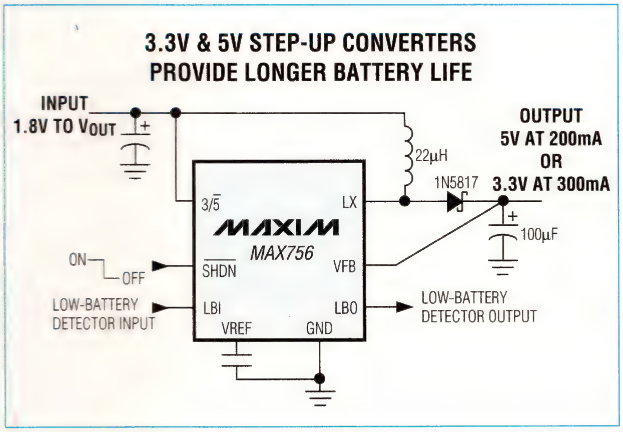

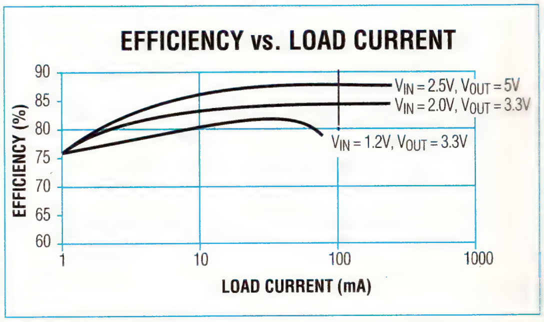

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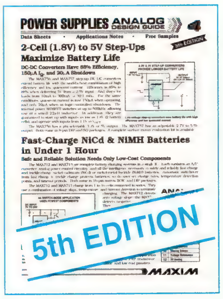
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CIRCLE NO. 84

Spice subcircuit simulates any second-order filter

Horace T Jones, Rockville, MD

The Spice subcircuit filter in **Listing 1**, along with the appropriate constants drawn from **Table 1**, simulates any second-order filter. The subcircuit in the **Listing** runs under MicroSim's (Irvine, CA) pSpice. To calculate the parameters that the subcircuit needs, begin with the classical transfer function for a filter

$$\frac{\text{VOUT}}{\text{VIN}} = \frac{S^2 * k2 + S * k1(Wp/Qp) + k0(Wp^2)}{S^2 + S(Wp/Qp) + Wp^2}$$

$$k1(Wp/Qp) = Wz/Qz$$

$$k0(wp^2) = Wz^2$$

where, because Spice accepts only unsubscripted Latin letters, Wp substitutes for the pole frequency ω_{POLE}, Qp for Q_{POLE}, and Fp for F_{POLE}. Similarly, Wz is the Spice-compatible symbol for the frequency of the zero ω_{ZERO}, and Qz for Q_{ZERO}.

Listing 1—Spice subcircuit filter

```
.SUBCKT FILTER  IN OUT PARAMS:Fp=1,Qp=1,k2=1,k1=1,k0=1
.PARAM Wp = {6.283185*Fp}, C = {PWR(Wp,-2)}
.PARAM  R = {Wp/Qp}, RQ = {Wp*Qp}
EBUF  1   0  IN  0  1
 R1    1   2  {R}
 C1    2   3  {C}
 L1    3   0  1
 R2    1   4  {RQ}
 L2    4   0  1
 C2    4   0  {C}
 R3    1   5  {R}
 L3    5   6  1
 C3    6   0  {C}
ESUM  OUT  0  VALUE = {k2*V(3) + k1*V(4) + k0*V(6)}
.ENDS
```

Table 1—Constants for filters

Filter type	k2	k1	k0	Gain
Lowpass	0	0	—	1.0 at dc
Bandpass	0	—	0	1.0 at Fp
Highpass	—	0	0	1.0 at infinity
Notch	—	0	(Fz/Fp)2	k0 at dc, 1.0 at infinity
Allpass	—	–1	—	1.0 for all frequencies
Bump	—	Note 1	—	1.0 at dc and infinity, |k1| at Fp

Note 1: Set k1 for the bump filter (or equalizer) equal to your desired gain at Fp. The magnitude of k1 may be greater than or less than 1.0. The amplitude response will be the same for +k1 or –k1, but the envelope delay will be different.

Note 2: "—" indicates that no entry is needed.

In a typical subcircuit call—in this case, a lowpass filter—you need to supply values only for the constants **Table 1** specifies. **Listing 1** supplies default values for k2, k1, and k0 on its first line.

X1 1 2 FILTER PARAMS: Fp = 1000, Qp = 2.2, K2 = 0, k1 = 0

The ASCII file, DI1347.TXT, attached to the message /DI_SIG #1347, contains a copy of the subcircuit. EDN

EDN BBS /DI_SIG #1347

To Vote For This Design, Circle No. 473

Simple circuit detects current pulses

Richard McGillivray, Grey Bruce Regional Health Centre, Owen Sound, Ontario, Canada

The pulse detector in **Fig 1** provides a visible indication of positive and negative current pulses. The pulses' amplitudes can vary from 20 to 150 mA. The pulses' durations can range from 10 to 40 msec, and their repetition rate can span 40 to 180 pulses/minute.

In **Fig 1**, the junction of the resistive divider connects to a bridge rectifier comprising diodes D_1 and D_2, and the LEDs D_3 and D_4. An N-channel JFET, Q_1, is the load for the bridge. The JFET provides a constant-current sink for the LEDs. Obviously, the JFET must have an I_{DSS} of less than the maximum LED forward current.

D_3 and D_4 indicate positive and negative pulses, respectively. The LEDs' brightness remains virtually constant over the specified range of input-current pulses. EDN

EDN BBS /DI_SIG #1353

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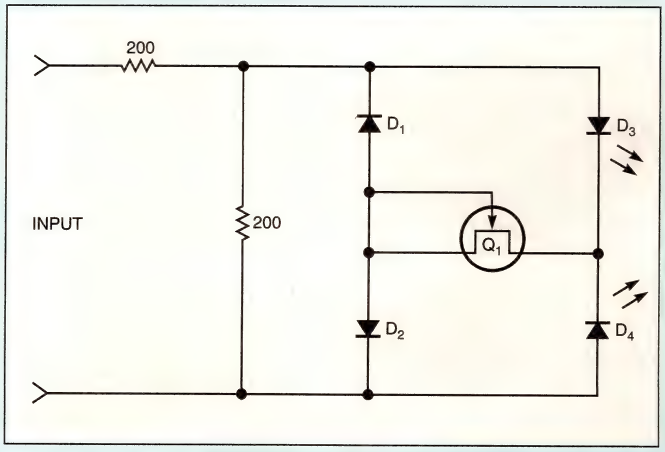

Fig 1—This pulse detector provides a visible indication of positive and negative current pulses.

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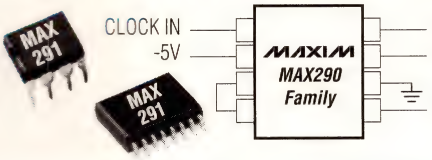

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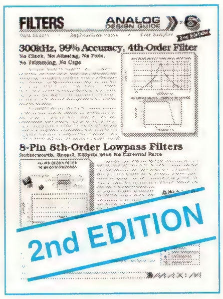
MAX294	Elliptic	0.1Hz - 25kHz	100:1	205dB/Octave Rolloff
MAX295	Butterworth	0.1Hz - 50kHz	50:1	No Passband Ripple
MAX296	Bessel	0.1Hz - 50kHz	50:1	Fastest Settling
MAX297	Elliptic	0.1Hz - 50kHz	50:1	133dB/Octave Rolloff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CIRCLE NO. 2

Feedback & Amplification

Design won't work

Mark Walsh's Design Idea #1275, "Diode implements reverse battery protection," *EDN*, September 30, 1993, pg 117, won't work. Reversing the battery still breaks down the base-emitter junction, with current flowing through the now forward-biased collector-base junction, potentially damaging the Darlington transistor and the load.
Ron Harrison, Grass Valley Group Inc
Box 1114, Grass Valley, CA 95945

I would like to offer an alternate solution to the problem of protecting a high-side solid-state switch from inductive transients (see Walsh's Design Idea #1275 referenced above). An inductive load can generate 1000 or more negative volts, depending on the size of the inductor. I doubt that Walsh's scheme really protects the Darlington. I suggest that paralleling the inductor with a diode limits the transient resulting from the magnetic field's collapse to one diode drop plus some minor amount of overshoot.
Glenn F Hoffstatter, 15600 Ocaso Ave
La Mirada, CA 90638

Changing a diode position in a battery circuit can save you some forward-drop voltage (see Walsh's Design Idea #1275 referenced above). However, in some situations, such as with a nonrechargeable lithium battery, this technique may not be advisable. Several safety agencies, such as UL, require two devices in series to prevent a hazard. Hazards can be reverse charging, forced charge, forced discharge or reverse-polarity installation. Two devices are required in the event of a fault in one device. If your circuit may be affected, you must keep this restriction in mind.
James Goedderz
Product Safety Engineer
Zenith Data Systems
211 Hilltop Rd
St Joseph, MI 49085

Software Shorts

TSR adds mouse to any application

K V Ramakrishnan, DRDO, NPOL
Cochin, Kerala, India

The TSR source code, documentation, and executable program in the ZIPfile DI1311Z.ZIP attached to **EDN BBS /DI_SIG #1311** lets you add mouse control to any PC application.

To Vote For This Design, Circle No. 475

This Software Short listing is too long to reproduce here. You can obtain the listings from the Design Idea Special Interest Group on EDN's bulletin-board system: (617) 558-4241, 300/1200/2400 8,N,1. From Main Menu, enter ss/DI_SIG, then rknnnnz, where nnnnz is the file referenced above.

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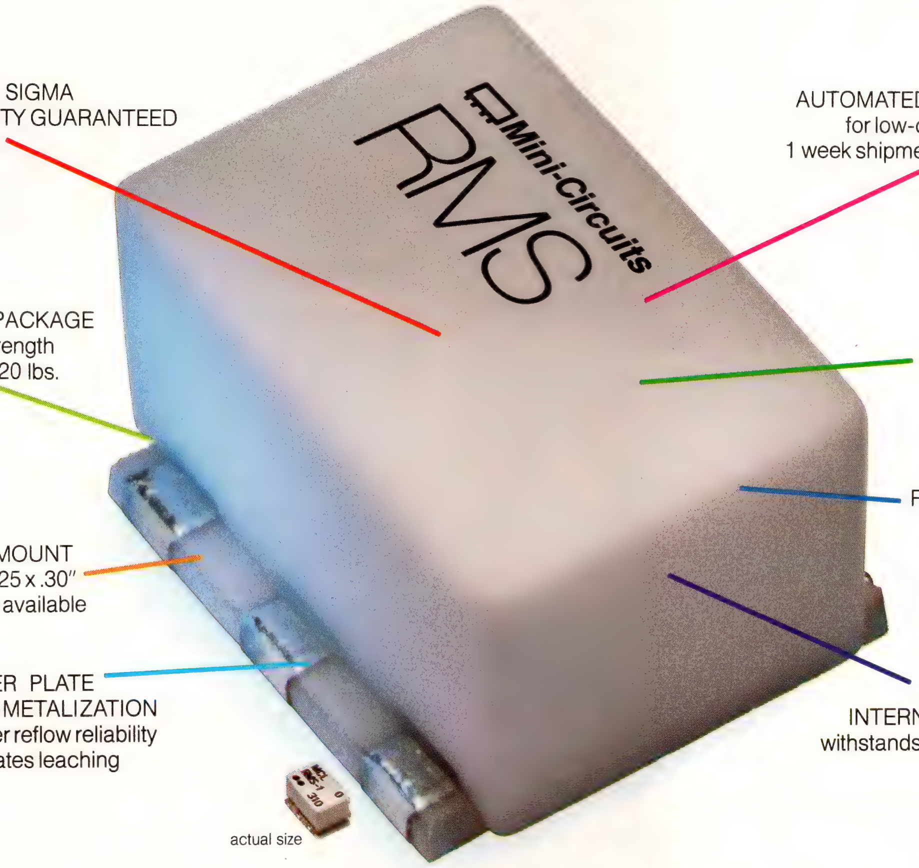

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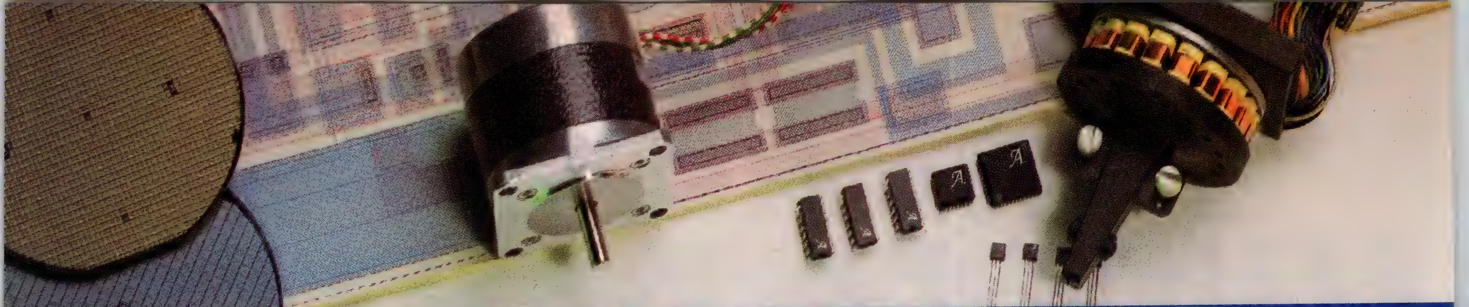
CIRCLE NO. 94



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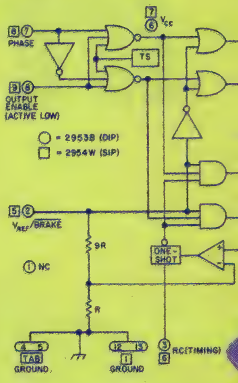

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Intended primarily to drive high-current, dot matrix printer solenoids, the UCN5829EB provides a complete driver function with minimum external parts.

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- 50 V Minimum Sustaining Voltage
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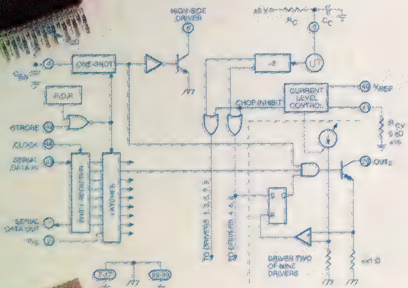

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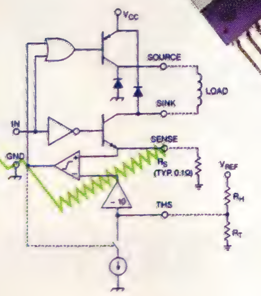

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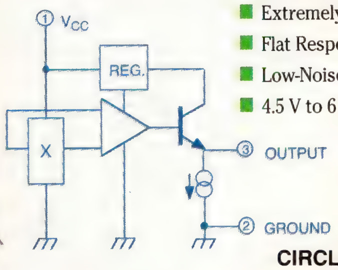

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Techniques illuminate backlit LCDs with high efficiency

Jim Williams, Linear Technology Corp

Getting a backlight LCD lamp to turn on is just the first step in the design process. Achieving and maintaining high efficiency requires attention to both circuit-design and physical-layout details.

A practical, 92%-efficient LCD-backlight design for cold-cathode fluorescent lamps (CCFLs) is a classic study of compromise in a transduced electronic system. Every aspect of the design is interrelated, and its physical embodiment is an integral part of the electrical circuit. The choice and location of the lamp, wires, display housing, and other items have a major effect on electrical characteristics. To achieve a practical, highly efficient LCD backlight, you must take the greatest care in every detail. Getting the lamp to light is just the beginning. (Note: The circuits and design principles that this article presents improve the efficiency of the author's initial LCD backlight design, which appeared in the October 29, 1992, issue of EDN (**Ref 1**).)

CCFLs are complex transducers, and many variables affect their ability to convert electrical current to light. Factors influencing conversion efficiency include the lamp's current, temperature, drive-waveform characteristics, length, width, gas constituents, and proximity to nearby conductors. These and other factors are interdependent, resulting in a complex overall response. **Fig 1** shows two curves of typical lamp characteristics: current (**Fig 1a**) and temperature (**Fig 1b**) vs emissivity. These curves don't correspond to any particular lamp but show general characteristics averaged over a dozen lamps from different manufacturers. These curves hint at the difficulty in predicting lamp behavior as operating conditions—including current and temperature as well as lamp voltage and length—vary.

The lamp's current and temperature are clearly critical to emission, although high electrical efficiency may not necessarily correspond to the highest optical efficiency. It is possible, for example, to construct a CCFL circuit with 94% electrical efficiency that produces less light than an approach with 80% electrical efficiency. Because of this fact, you must often perform both electrical and photometric evaluation of a circuit.

Furthermore, a lossy display enclosure or excessive high-voltage-wire lengths can severely degrade the performance of a very well matched lamp-circuit combination. Display

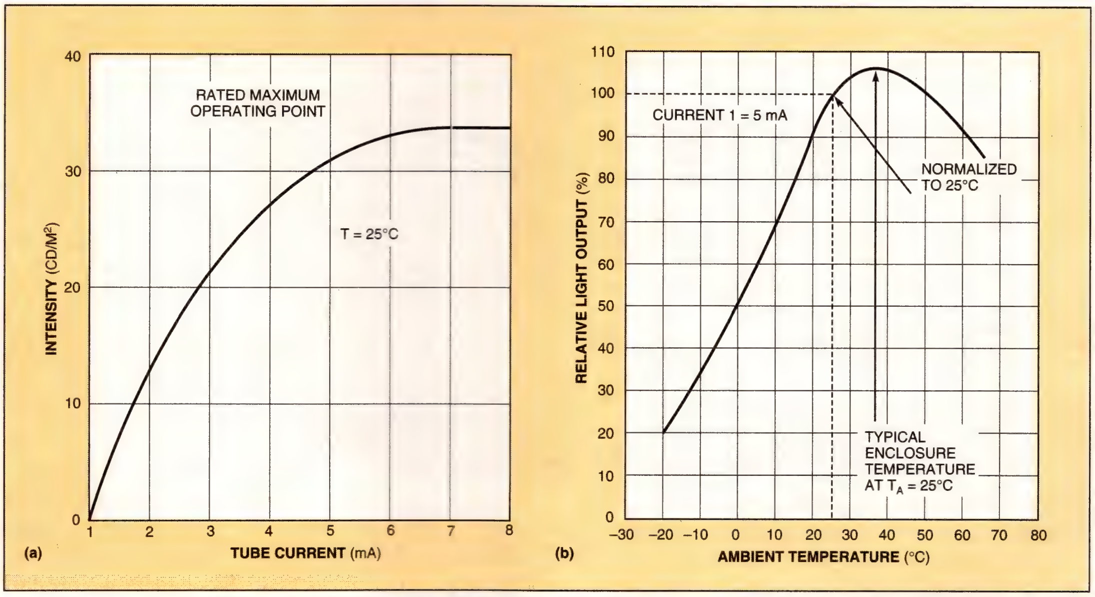


Fig 1—A typical lamp profile of current vs intensity (a) shows a curve that flattens badly above 6 mA. Ambient temperature also has a decided effect on the lamp's emissivity (b).

enclosures with too much conducting material near the lamp have huge losses due to capacitive coupling. A poorly designed display enclosure can easily degrade efficiency by 20%. High-voltage wire runs typically cause 1% loss/in. of wire.

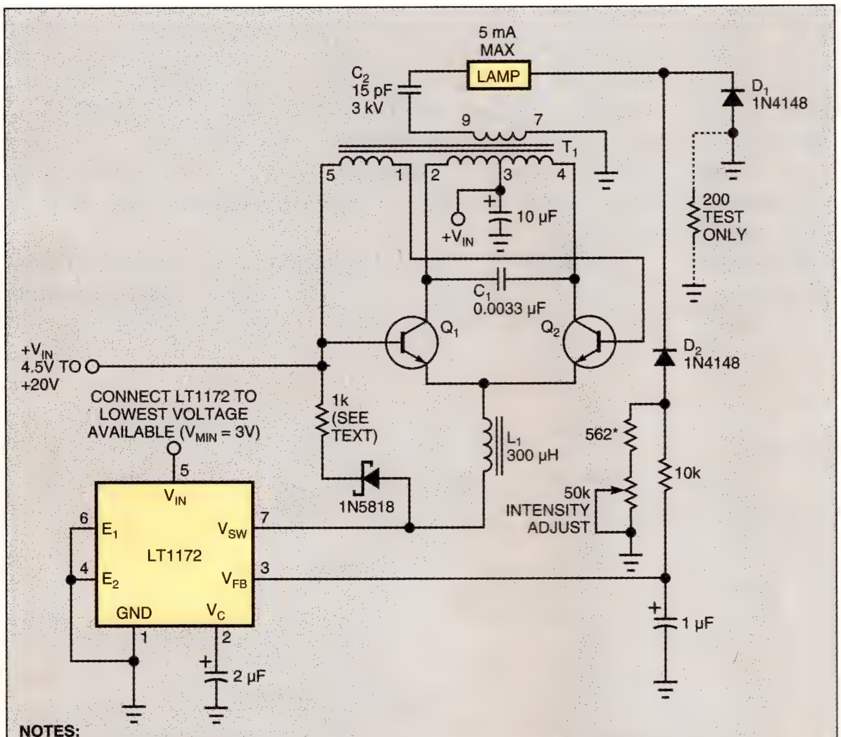
Because the LCD backlight can take as much as 50% of a computer's power, any efficiency improvement is noteworthy. The circuit in **Fig 2** improves the efficiency of the original circuit (**Ref 1** and **Ref 2**) by 6 to 88%. However, if you don't have a low-voltage supply available in the display area to drive the LT1172's V_{IN} pin, this efficiency figure degrades by about 3%. The efficiency improvement is primarily due to the transistor's higher gain and lower saturation voltage. You must carefully select the base-drive resistor's value—nominally 1 kΩ—to provide full V_{CE} saturation without inducing base overdrive or beta starvation.

As in the original circuit, the lamp intensity is continuously and smoothly variable from zero to full intensity, and the input voltage range remains the same at 4.5 to 20V.

The details of the circuit's operation are the same as described in **Ref 1** and **Ref 2.** In essence, the circuit is a current-sink-driven resonant Royer converter (**Ref 3**). The LT1172 and L_1 form a switch-mode current sink. Q_1, Q_2, T_1, and associated components comprise the resonant Royer converter. Rectified feedback from the Royer converter's output via D_2 closes constant-current a loop back to the LT1172's V_{FB} pin.

In addition to improving efficiency, this general circuit approach has other advantages: tight line regulation and extended dimming range. Additionally, the circuit enhances the lamp's operating life because current can't increase as the lamp ages. The circuit's 0.1% line regulation is notably better than that of some other approaches. Tight regulation prevents the lamp intensity from varying when abrupt line changes occur, which typically happens when you connect a battery-powered apparatus to an ac-powered charger. The circuit's excellent line regulation stems from the fact that T_1's drive waveform never changes shape as input voltage varies. This characteristic permits the simple 10-kΩ to 1-µF RC network to produce a consistent response. The RC averaging characteristic has serious error compared to a true rms conversion, but the error is constant and the 562Ω shunt's value calibrates out the error.

The circuit in **Fig 3** is similar to the one in **Fig 2** but uses a transformer with lower copper and core losses to increase efficiency to 92%. The tradeoff is slightly larger transformer size. Value shifts in C_1, L_1, and the base-drive resistor reflect different transformer characteristics. This circuit also features a dc or pulse-width-controlled dimming input and shutdown via Q_3.



NOTES:
C_1 = MUST BE A LOW-LOSS CAPACITOR
METALIZED POLYCARB
WIMA FKP2 OR MKP-20 (GERMAN) RECOMMENDED
T_1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L_1 = COILTRONICS CTX300-4
Q_1, Q_2 = ZETEX ZTX849 OR ROHM 2SC5001

* = 1% FILM RESISTOR

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Fig 2—This current-sink-driven resonant Royer converter powers a cold-cathode fluorescent lamp with 88% efficiency. The circuit's added benefits are 0.1% line regulation and a wide dimming range.

Keep several points in mind when observing the operation of these circuits. Only a wideband, high-voltage probe that's fully specified for this type of measurement can monitor T_1's high-voltage secondary. Most scope probes break down and fail to make this measurement (**Ref 4**). To read T_1's output, Tektronix probes types P-6007 and P-6009 are acceptable in some cases, but types P-6013A and P6015 are preferable.

Obtaining and verifying high efficiency takes diligence. The values in **Fig 2** and **Fig 3** for C_1 and C_2 are typical for achieving high efficiency and vary for specific types of lamps. An important realization is that the term "lamp" includes the *total* load seen by the transformer's secondary. This load, reflected back to the primary, sets the transformer's input impedance. The transformer's input impedance forms an integral part of the LC tank circuit that produces the high-voltage drive. Thus, you must optimize circuit efficiency by arranging the wiring, display housing, and physical layout *exactly* the same way they will be built in production. Deviations from this procedure result in lower efficiency than otherwise possible.

In practice, a first-cut efficiency optimization with best-guess lead lengths and the intended lamp in its display housing usually produces results within 5% of the achievable figure. When the production circuit's physical layout is set, you can fix the values for C_1

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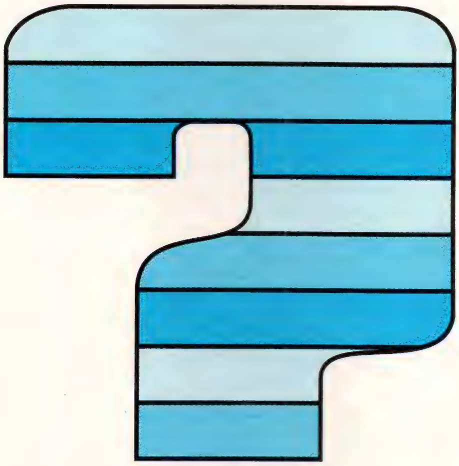

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TVP3020 Color Depth and Resolution

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1024 x 768	85 MHz	16 million (24-bit true color)	64K
1280 x 1024	135 MHz	64K (16-bit true color)	256
1600 x 1280	200 MHz	64K (16-bit true color)	N/A

System Requirements	TVP3020 Offers
• More colors at high resolution	• 64-bit pixel bus
• Simplified VGA interface	• Separate VGA port
• High-screen resolution	• Dot clock up to 200 MHz
• Faster graphics performance	• Hardware cursor
• Lower cost external TTL PLL	• Internal frequency doubler
• More accurate color rendition	• Gamma-corrected true color
• Control of overlays for multimedia	• Color-key switching

The TVP3020 allows flexibility in designing photo-realistic graphics systems up to 16 million colors. It enables you to support 24-bit true color at 1024 x 768 as well as 16-bit true color at both 1280 x 1024 and 1600 x 1280 with a single design.†

TVP3020

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CIRCLE NO. 140

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and C_2. C_1 sets the circuit's resonance point, which varies to some extent with the lamp's characteristics. C_2 ballasts the lamp, effectively buffering its negative-resistance characteristic. Small values of C_2 provide the most load isolation but require relatively large transformer output voltage for loop closure. Large C_2 values minimize transformer output voltage but degrade load buffering.

Components' values depend on the lamp

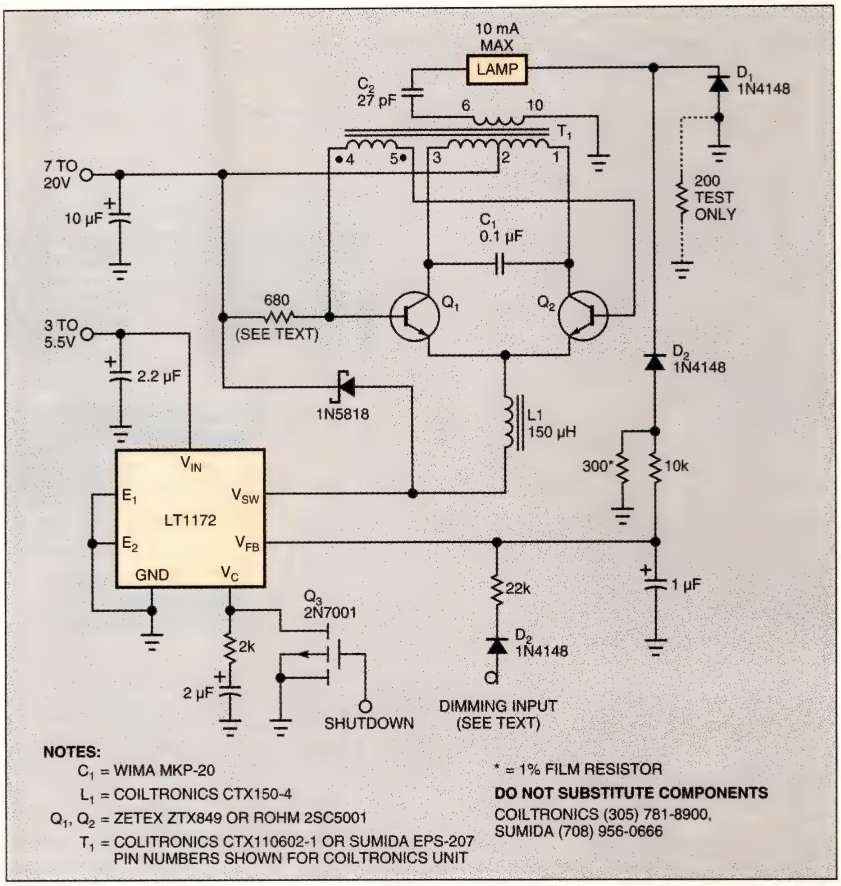
The best values for C_1 and C_2 depend on the specific lamp you use. Some interaction occurs between the two capacitors, but generalized selection guidelines are possible. Typical values for C_1 are 0.01 to 0.15 μF. C_2 usually ends up in the 10- to 47-pF range. C_1 must be a low-loss capacitor; substituting a poor-quality dielectric for C_1 can easily degrade efficiency by 10%.

Before selecting a capacitor, set the value of the Q_1 to Q_2 base-drive resistor to a value, such as 470Ω, which ensures saturation. Next, select C_1 and C_2 by trying different values for each and iterating toward best efficiency. During this procedure, monitor IC_1's feedback pin, which should be at 1.23V, to ensure that the loop is closed. Several trials usually produce the optimum C_1 and C_2 values. The highest efficiencies are not necessarily associated with the most esthetically pleasing waveshapes, particularly at Q_1, Q_2, and the output.

Now you should optimize the base-drive resistor's value. This resistor's value, which is nominally 1 kΩ, should provide full V_{CE} saturation without inducing base overdrive or beta starvation. Using full lamp power, the point at which the collector current peaks determines the optimum value. The resistor should equal the largest value that ensures saturation for worst-case transistor beta. You can verify this condition by varying the resistor about the ideal value and noting the small variations in input supply current. The minimum obtainable current corresponds to the best beta-vs-saturation tradeoff. In practice, supply current rises slightly on either side of this point. This double-value behavior is due to excessive base-drive or saturation losses, which degrade efficiency.

Other issues influencing efficiency include the lamp's wire length and energy leakage. The high-voltage side of the lamp should have the smallest practical lead length. Excessive length results in radiative losses, which can easily reach 3% for a 3-in. wire. Similarly, to prevent energy leakage, which can degrade efficiency by 10%, metal should neither contact nor be close to the lamp.

Finally, a custom-designed lamp affords the best possible results. A jointly tailored lamp-circuit combination permits precise optimization of circuit operation to yield the highest efficiency. EDN



NOTES:
C_1 = WIMA MKP-20
L_1 = COILTRONICS CTX150-4
Q_1, Q_2 = ZETEX ZTX849 OR ROHM 2SC5001
T_1 = COLITRONICS CTX110602-1 OR SUMIDA EPS-207
PIN NUMBERS SHOWN FOR COILTRONICS UNIT

* = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS
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Fig 3—Using a larger transformer that has lower copper and core losses, this cold-cathode fluorescent-lamp supply features 92% efficiency and adds shutdown- and dimming-control inputs.

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3. Bright, Pittman, and Royer, "Transistors as On-Off Switches in Saturable Core Circuits," *Electrical Manufacturing*, Technomic Publishing, Lancaster, PA, December, 1954.

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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Lab at the Massachusetts Institute of Technology. A former student at Wayne State University (Detroit, MI), Jim enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

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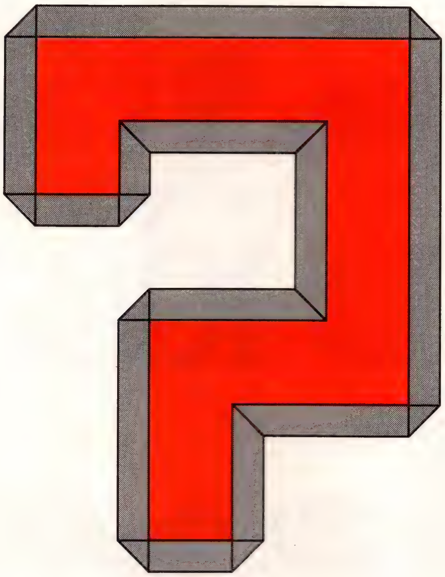

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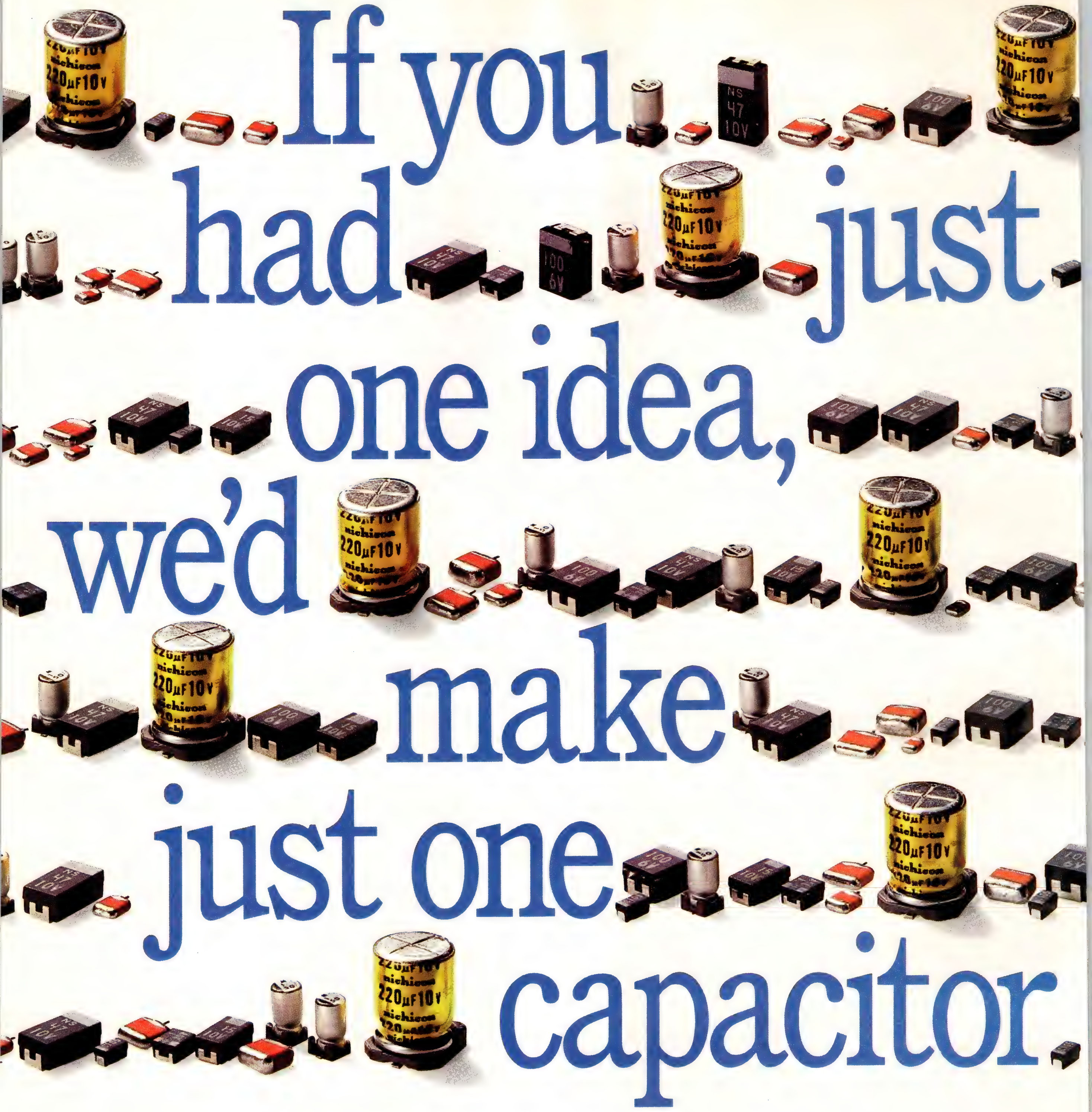

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CIRCLE NO. 97

Phase compensation counteracts op-amp input capacitance

Jerald Graeme, Burr-Brown Corp

Although op amps are mature devices, many designers often ignore the effects of input capacitance on frequency stability. A bode plot analysis lets you add compensation capacitors to counteract poles and zeros caused by an op amp's input capacitance.

An op amp's input capacitance can often be the bugaboo that prevents the frequency stability of a circuit. The reason is that input capacitance along with the resistive feedback network creates a pole in an inverting amplifier that introduces phase lag in the open-loop response. In noninverting op amps, the input capacitance can produce a zero in the closed-loop response, which causes high-frequency peaking, which can degrade common-mode rejection. Knowledge about phase-compensation techniques can help you counteract these deleterious effects of an op amp's input capacitance.

Fig 1 illustrates an inverting amplifier with some typical values for the input capacitance. C_{id} represents the differential capacitance between the amplifier's two inputs. The two C_{icm} components represent the common-mode input capacitance for each op-amp input to ground. In the inverting configuration, two of the three input capacitances shunt the feedback network. A capacitor in the feedback path C_f compensates for the effects of the input capacitance. To examine the effects of the input capacitance when C_f is 0, consider the uncompensated feedback voltage divider:

$$\beta = \frac{\beta_0}{1+(R_1 \| R_2)C_i s},$$

where $\beta_0=R_1/(R_1+R_2)$ and $C_i=C_{id}+C_{icm}$. The op-amp input capacitance introduces a feedback pole at $f=1/2\pi(R_1 \| R_2)C_i$.

The significance of the feedback pole produced by C_i on frequency stability depends on the values of the feedback resistors. Large resistor values and op amps with wide open-loop bandwidths cause stability concerns. The addition of C_f in the feedback path introduces a zero to compensate for the feedback pole. **Fig 2** is a bode diagram that demonstrates the stabilizing effect of C_f. The interception of the op amp's open-loop gain curve and the $1/\beta$ response determine the circuit's frequency stability. The $1/\beta$ response is:

$$1/\beta = \frac{1+(R_1 \| R_2)(C_1+C_f)s}{1+R_2C_f s}(1/\beta_0),$$

where $\beta_0=R_1/(R_1+R_2)$.

Bode analysis finds compensation point

The bode diagram shows a rise in the frequency response of $1/\beta$ due to the zero at $f_z=1/2\pi(R_1 \| R_2)(C_i+C_f)$. Without the pole in the $1/\beta$ response at $f_p=1/2\pi R_2C_f$, the open-loop gain A_{OL} and the $1/\beta$ curve would intersect with a 40-dB/decade slope difference, which would produce 180° phase shift at the intercept point and loop oscillations. Placing f_p at the intercept point introduces 45° of phase correction and extends the

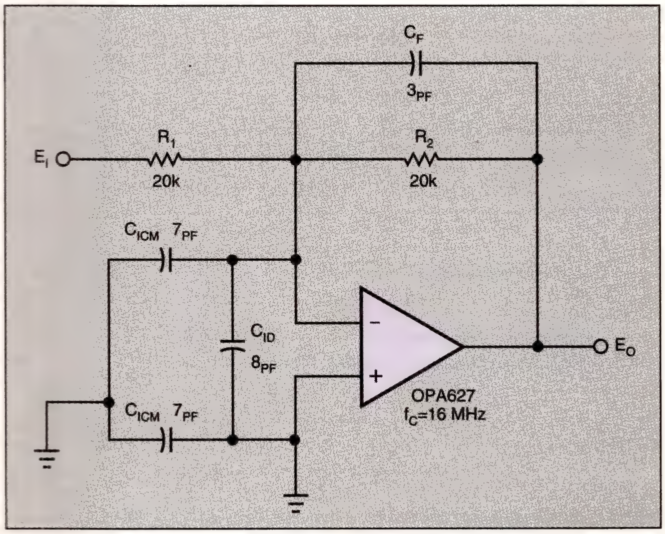

Fig 1—A noninverting op amp's input capacitance plagues its frequency stability. The op-amp capacitance is shown here as the common-mode capacitance (C_{icm}) for each input and the differential capacitance between the inputs (C_{id}).

closed-loop bandwidth to f_i. The phase shift at the intercept point reduces from 180 to 135°, producing a 45° phase margin. Placing the f_p closer to the f_z would further increase the phase margin. However, because C_f shunts the feedback resistor, the C_f increase required for this phase margin would restrict the inverting circuit's bandwidth.

To quantify f_i and C_f using geometric analysis, note the triangle in the bode diagram formed by the rise in the $1/\beta$ response, the fall in the A_{OL} response, and the projected dash extension of the $1/\beta_0$ curve. The intercept point, f_i, lies midway between the f_z and B_0f_c endpoints of the base of the triangle. The logarithm of the midpoint is given as Log f_i=(Log f_z+Log β_0f_c)/2. Solving for f_i yields:

$$f_i=\sqrt{(f_z\beta_0 f_c)}=\sqrt{[f_c/2\pi R_2(C_i+C_f)]}.$$

Setting $f_p=f_i=1/2\pi R_2C_f$ yields the value of the compensation capacitor, C_f. Another convenient way to determine C_f is to assume a fictitious capacitor that creates the amplifier crossover frequency, f_c. The fictitious capacitor is given by $C_c=1/2\pi R_2f_c$. Solving for the compensation capacitor in terms of the fictitious capacitor yields:

$$C_f=(C_c/2)[1+\sqrt{(1+4C_i/C_c)}],$$

where

$$C_c=1/2\pi R_2 f_c \text{ and } C_i=C_{id}+C_{icm}.$$

For a crossover frequency of f_c=16 MHz and a total input capacitance of C_i=14 pF, the compensation capacitor is C_f=3 pF.

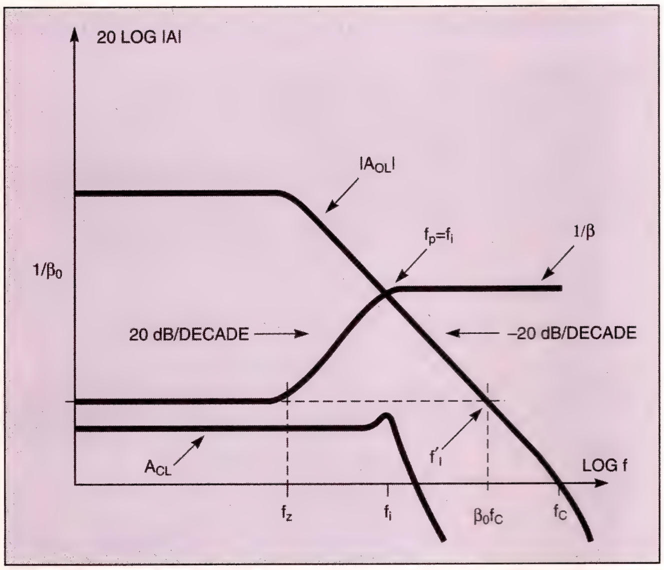

Fig 2—The closed-loop response of an inverting amplifier shows the open-loop response and the $1/\beta$ response closing at a rate of 40 dB/decade without compensation. The compensation capacitor introduces a pole at f_p to decrease the rate of closure and increase the phase margin to 45°.

The test to determine whether C_f for the noninverting amplifier is needed comprises the following steps. First, compute $f_z=1/2\pi R_1||R_2C_i$, where $C_i=C_{id}+C_{icm}$. Compare the result with β_0f_c, where β_0=/R_1+R_2 and f_c is the crossover frequency of the op amp. If f_z is greater than β_0f_c, then no compensation is required and there is no peaking in the closed-loop response. When f_z is less than β_0f_c, however, you calculate the compensation capacitor by:

$$C_f=(C_c/2)[1+\sqrt{(1+4C_i/C_c)}]$$

where

$$C_c=1/2\pi R_2 f_c \text{ and } C_i=C_{id}+C_{icm}.$$

For the component values shown in **Fig 1**, C_i=15 pF and $R_1||R_2$=10 kω, which makes f_z=1.06 MHz. Also β_0=0.5 and f_c=16 MHz, so the calculated value for β_0f_c=8 MHz. Because $f_z<\beta_0f_c$, the circuit requires phase compensation. In this case, the wide bandwidth of the OPA627 op amp and the large value of 20 kω for feedback resistors contribute to the need for compensation. The closed-loop bandwidth for the circuit is BW=1.4f_i. For the values shown, f_i=2.7 MHz, so the BW=3.8 MHz.

Watch out for peaking in noninverters

In the noninverting op-amp configuration (**Fig 3**), one of the input capacitors (C_{icm}) shunts the feedback resistor (R_1). Although the feedback factor β is the same as the inverting amplifier, at high frequencies C_{icm} and R_1 introduce a zero in the closed-loop response, which causes peaking. This effect does not occur in the inverting configuration because the inverting input is at a virtual ground. The phase-compensation capacitor C_f can also compensate for the peaking in the noninverting configuration. An appropriate choice of C_f cre-

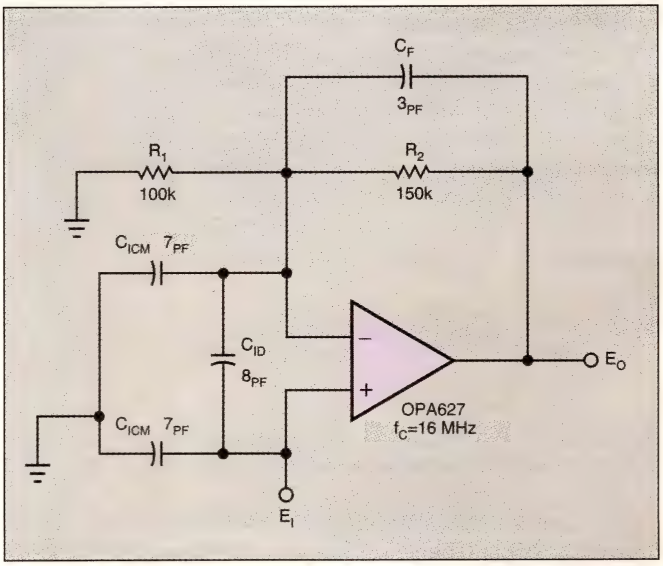

Fig 3—In the noninverting amplifier, the common-mode input capacitance C_{icm} from the inverting input to ground shunts R_1, which can cause peaking in the closed-loop response at high frequencies.

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ates a pole that cancels the zero produced by C_{icm}. Cancellation occurs when $C_f \times R_2 = C_{icm} \times R_1$. Solving for C_f:

$$C_f = (R_1/R_2)C_{icm}.$$

To compensate for peaking in the closed-loop response, use:

$$C_f = (R_1 / R_2)C_{icm}.$$

Because the calculated capacitance for peaking compensation is a larger value than the calculated phase-compensation capacitor, you can use the larger value to extend the closed-loop bandwidth.

How well the pole cancels the zero depends on the variation in the input capacitance due to production variances and voltage sensitivity. C_{icm} is dependent on voltage; therefore, the signal level at e_1 can introduce high-frequency distortion, which affects the frequency compensation. However, the input-capacitance variation is generally small, so high-frequency distortion is generally slight whether or not you employ a compensation capacitor.

Fig 4 is a bode diagram for a compensated noninverting amplifier. The figure shows the op amp's open- (A_{OL}) and closed-loop (A_{CL}) responses, along with the 1/β response curve. The dashed curve superimposes the 1/β response for the previously considered inverting amplifier. Using a larger compensation capacitor C_f than the noninverting case eliminates any overshoot in the closed-loop response.

The interception of the 1/β curve and the A_{OL} curves determines the closed-loop bandwidth $B_H f_c$. The closed-loop bandwidth f_i' for the noninverting amplifier is wider than the inverting amplifier f_i. Also note that the noninverting compensation capacitor levels off the 1/β curve at a lower frequency than the intercept point with the A_{OL} curve. The noninverting closed-loop bandwidth is given as:

$$BW = \beta_H f_c = \frac{C_i f_c}{C_i + C_f},$$

where

$$C_i = C_{id} + C_{icm}.$$

For the values shown in the figures, the bandwidth for the noninverting amplifier is 13 MHz vs 3.8 MHz for the inverting amplifier.

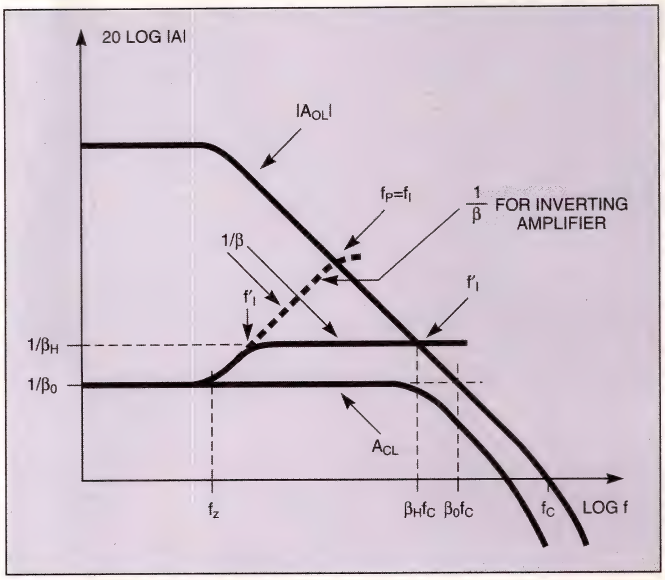

Fig 4—To compensate the noninverting amplifier for peaking, choose the compensation capacitor so that it creates a pole in the 1/β response that cancels the zero in the 1/β curve for the inverting amplifier.

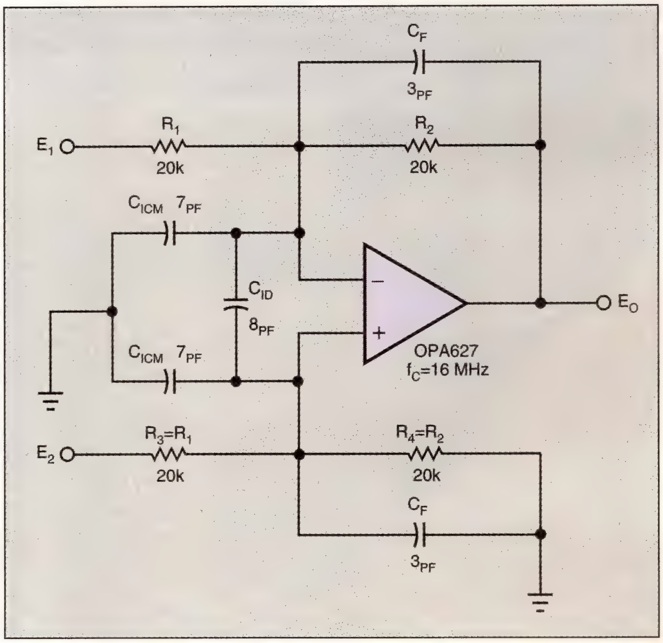

Fig 5—Compensating a difference amplifier is a compromise between the inverting and noninverting configurations. You need an additional pole at the noninverting input to the op amp to cancel a zero in the feedback factor.

Differential op amps are a mixture

A differential op-amp configuration poses conflicting phase-compensation demands because of the combined effect of the noninverting and inverting configurations. Fortunately, a judicious choice of circuit resistance can compensate for the conflict. **Fig 5** depicts a difference amplifier with the op amp's input capacitances brought out for circuit analysis. At first glance, it appears that the value of the feedback compensation capacitor C_f conflicts with frequency stability and gain-peaking compensation. In addition, the value of C_{icm} in parallel with R_4 provides an extra pole to the e_2 path that doesn't occur in the e_1 path.

Analysis of the circuit's closed-loop response, however, shows that the compensation for gain peaking resolves the phase-compensation difference for both paths to the op amp. With no feedback compensation capacitor (C_f=0), the closed-loop response is given by:

$$A_{CL} = -\frac{R_2}{R_1} e_1 + \frac{R_4(R_1+R_2)}{R_1(R_3+R_4)} \, \frac{1+(R_1 \| R_2)C_{icm}s}{1+(R_3 \| R_4)_{C_{icm}} s} e_2.$$

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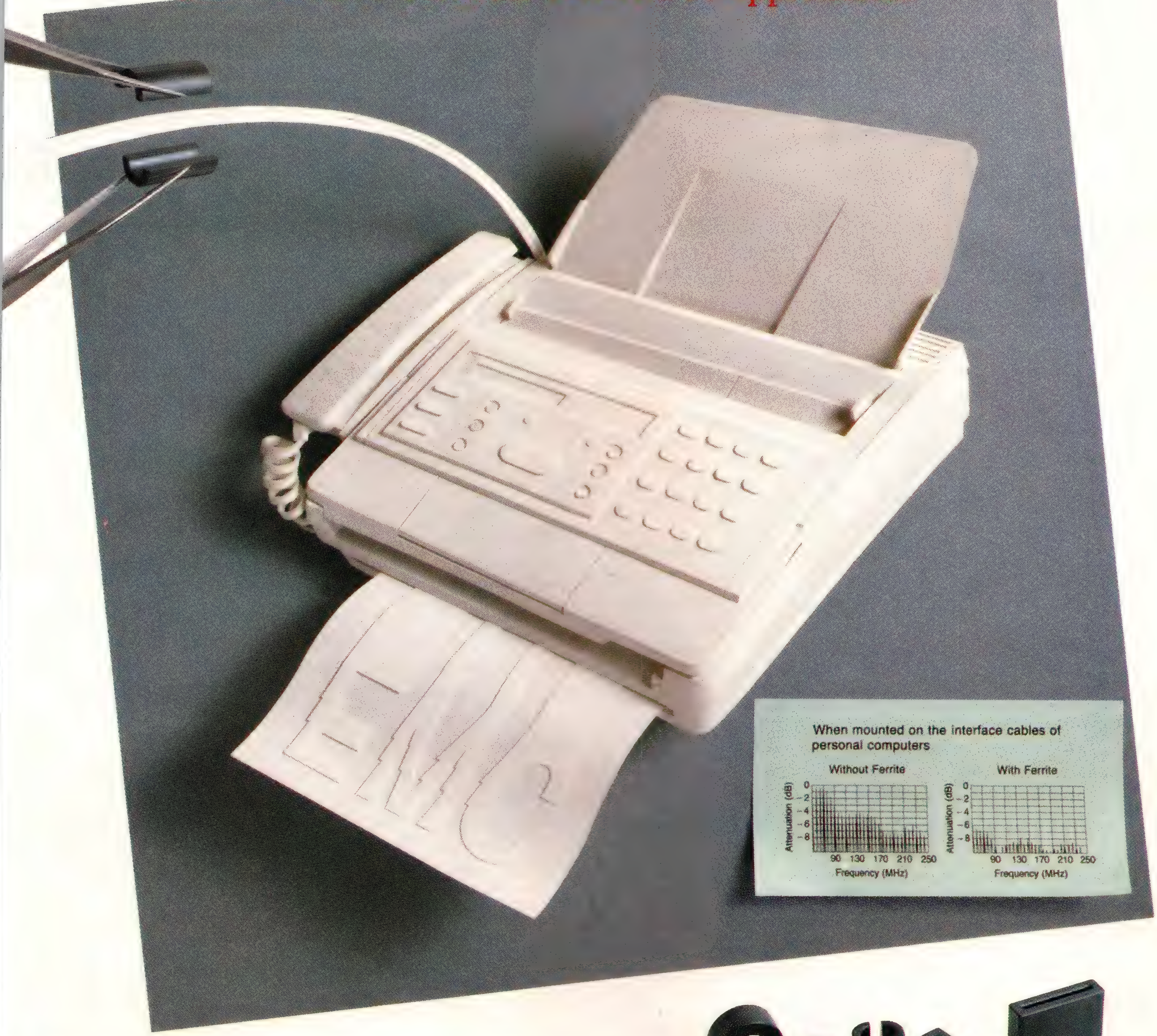

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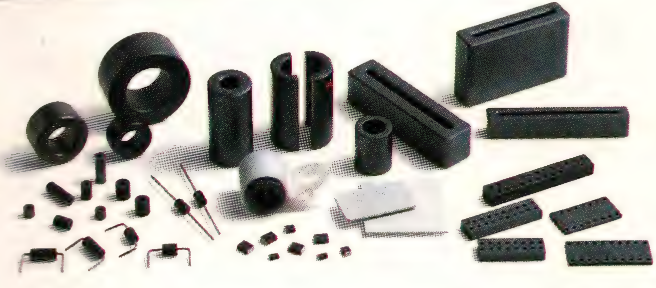

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To balance the dc gain for each input path, set the circuit resistor ratios so that $R_4/R_3=R_2/R_1$. Maintaining these resistor ratios reduces the closed-loop gain to:

$$A_{CL}=-\frac{R_2}{R_1}e_1+\frac{R_2}{R_1}\,\frac{1+(R_1\|R_2)C_{icm}s}{1+(R_3\|R_4)C_{icm}s}\,e_2.$$

When s=0, the dc gain for both input paths are the same. However, the ac closed-loop response for the e_2 path has a pole at $f_{p2}=1/2\pi(R_3\|R_4)C_{icm}$ and a zero at $f_{z2}=1/2\pi R_1\|R_2C_{icm}$. Although both singularities depend on C_{icm}, the capacitances are at the opposite op-amp inputs. Because the capacitors are closely matched, you can make the pole and zero cancel by allowing $R_3=R_1$ and $R_4=R_2$. Under these conditions, the closed-loop gain is:

$$A_{CL}=-\frac{R_2}{R_1}e_1+\frac{R_2}{R_1}e_2.$$

The previous closed-loop analysis of the difference amplifier ignores the effect of the op amp's open-loop response (A_{OL}), which must be phase-compensated. To phase-compensate the difference amplifier, you must bypass R_2 with C_f as described for the inverting and noninverting amplifiers. Although both the e_1 and e_2 gain paths experience the same pole at $1/2\pi R_2C_fs$, the feedback capacitor alters the f_{z2} zero for the e_2 path without equivalently affecting a zero in the e_1 path. The uncompensated f_{z2} zero is caused by the resistive feedback network of $R_1\|R_2$ reacting with C_{icm} capacitor at the negative op-amp input. By bypassing R_2 with a compensation capacitor C_f, you modify the f_{z2} zero to be $1/2\pi(R_1\|R_2)(C_{icm}+C_f)$.

A second capacitor does the trick

The modified f_z no longer cancels the pole at $f_{p2}=1/2\pi(R_1\|R_2)C_{icm}$. To realign the pole and zero cancellation, you must bypass R_4 with an equivalent compensation capacitor equal in value to C_f. The second compensation capacitor generates a pole at $f_{p2}=1/2\pi(R_1\|R_2)(C_{icm}+C_f)$, which effectively cancels the zero at f_{z2}. The resulting closed-loop gain is given as:

$$A_{CL}=\frac{R_2}{R_1(1+R_2C_fs)}(e_2-e_1).$$

The pole-zero cancellation described for the difference amplifier suggests an alternative compensation method for the noninverting case. Grounding the e_1 input for the difference amplifiers converts the circuit into a noninverting configuration. However, the input impedance is R_3+R_4, which is not as large as the input impedance for the connection shown in **Fig 3**. However, because there is only gain to the e_2 path in the noninverting amplifier, you need only the resistance ratio $R_3\|R_4=R_1\|R_2$ to maintain the pole and zero cancellation. To accommodate large source impedances (R_s), make $R_4=\infty$ and $R_3=R_1\|R_2-R_s$ to achieve a large input impedance.

The previous analysis of the noninverting amplifier in **Fig 3** ignored the effect of the source impedance's reacting with the C_{icm} capacitance, causing an uncompensated pole in the closed-loop response. The addition of R_3 and the addition of C_f from the op-amp noninverting input to ground provides compensation for this pole, as described in the difference amplifier configuration. The pole-zero matching also removes a potential distortion effect. The voltage levels at the op-amp inputs cause C_{icm} to vary slightly; however, the matching of the pole and zero causes the distortion products to cancel.

Equal signal voltages on the two C_{icm} capacitors maintain the pole-zero cancellation, which removes any high-frequency distortion to which the circuit in **Fig 3** is susceptible. In addition, by making the impedances for the dc currents for each op-amp input the same, you minimize the effect of input offset currents on the amplifier's overall output offset voltage.

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Author's biography

Jerry Graeme, a prolific contributer to EDN, manages instrument-component design for Burr-Brown Corp in Tucson, AZ. At Burr-Brown he has designed many analog ICs. He holds a BSEE from the University of Arizona and an MSEE from Stanford University. In his leisure time he enjoys scuba diving, photography, and woodworking.

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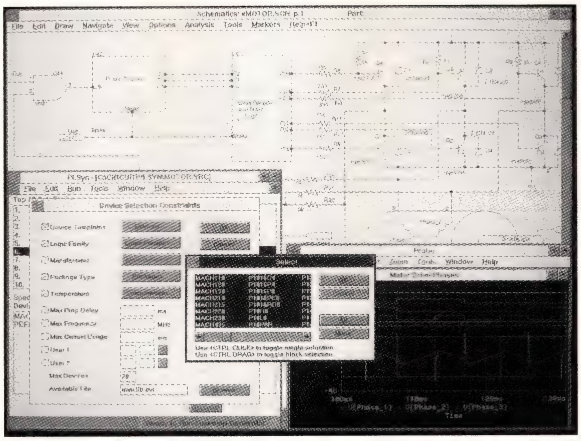
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The successful RTOS is available for almost all DSPs for use in embedded systems, and the new version makes it available for use in PCs. It lets multiple Windows-based applications have access to the DSP simultaneously; the applications are transparent to each other.

The RTOS includes a standard DSP application-programming interface (API) for Windows-based applications, which lets you create programs that work with other applications and a variety of DSP hardware. The product provides reference designs for Analog Devices, Texas Instruments, and Motorola DSPs.

The SPOX multimedia platform resides within the DSP, which can be on the mother board or on an add-in card. It works with Microsoft's SPOX-based DSP API, which runs under Windows on a PC.

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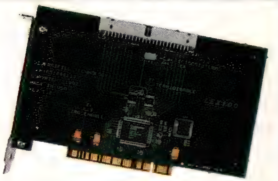

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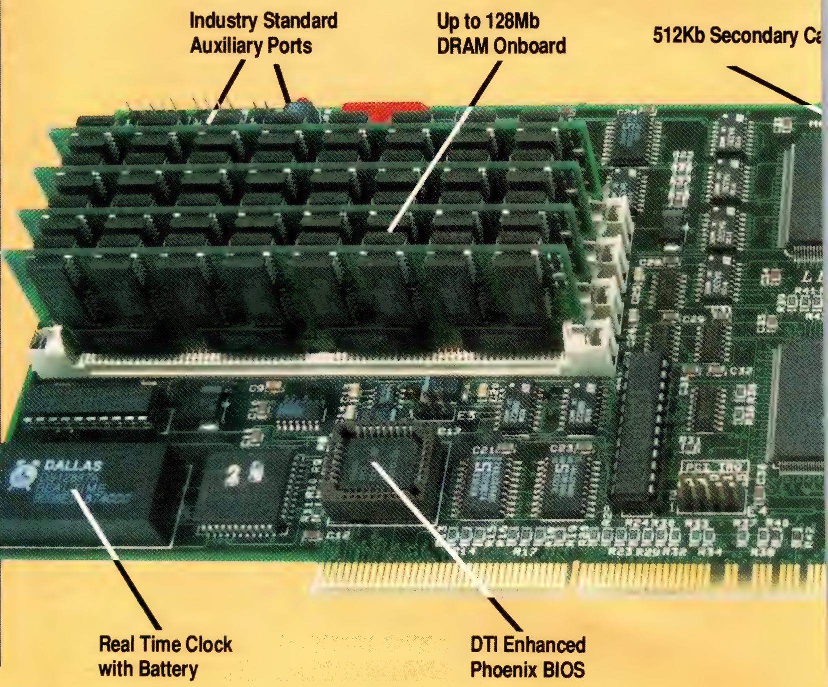
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ging tool), multimedia device drivers, and a reference-board support package. Prices start at $15,000. OEM runtime licenses start at $1.—**David Shear**

Spectron Microsystems, Goleta, CA. (805) 968-5100. **Circle No. 494**

Microsoft Corp, Redmond, WA. (206) 882-8080. **Circle No. 495**

Debug DSP over LAN from your workstation

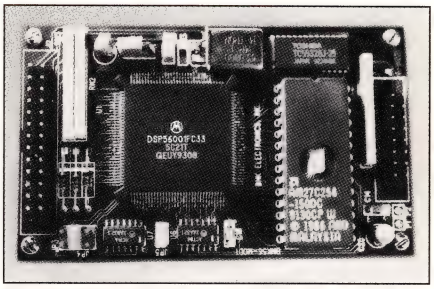
Spectrum Signal Processing has introduced the Remote Ethernet Debugging System (REDS), which lets you debug your DSP-based project over Ethernet. The workstation connects to a VMEbus-based target system via a gateway board, allowing Texas Instruments' DSP software tools to run on a Sun workstation as if directly connected to the target.

The gateway board provides a path from the workstation to JTAG controllers on the board. The JTAG controllers communicate with the TMS320C40 DSP chips in the VME chassis. You can use the TI software tools as if the JTAG controller were in the workstation. The system does not require a PC or any external hardware.

REDS costs $8500, including the gateway board. It comes on a Sun tape cartridge with the client and server applications.—**David Shear**

Spectrum Signal Processing Inc, Burnaby, BC, Canada. (604) 421-5422. **Circle No. 496**

DSP56001 development board costs $199



The BNK56-MOD1 board is the heart of the MM56001 low-cost development system. The board includes a Motorola DSP56001, EPROM, and 96 kbytes of SRAM (under the EPROM).

The MightyMight 56001 (MM56001) development system costs $199. The device is based on the BNK56-MOD1 board, which contains a 33-MHz Motorola DSP56001 DSP chip, 96 kbytes of zero-wait-state SRAM, and 32 kbytes of EPROM. You can use the board stand-alone or for development.

The system also includes the BNK56-MOD7 controller module for development. It has an RS-232C interface, which allows communication between the BNK56-MOD1 and the host. It also includes a debugger and a C utility library.

In the host-computer/debug mode, the debugger has full control over the DSP. You can view and modify registers and memory, single step, set breakpoints, and download code. A C compiler and assembler are available now, and analog-I/O options will be available soon.—**David Shear**

BNK Electronics Inc, Englewood Cliffs, NJ. (201) 894-5905. **Circle No. 497**

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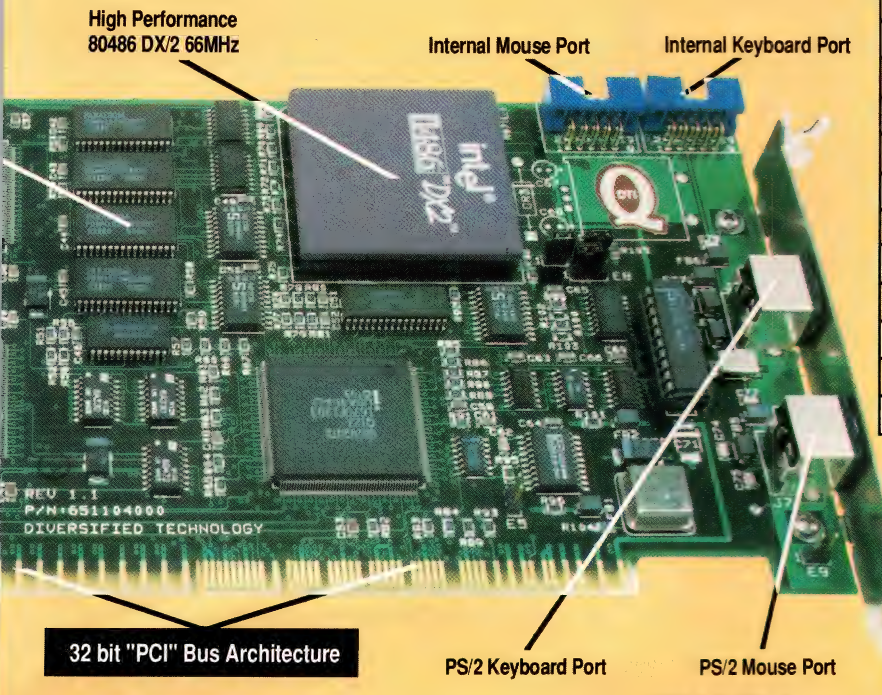

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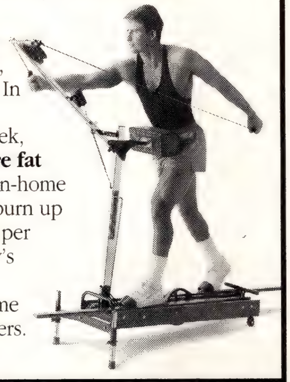

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CIRCLE NO. 9

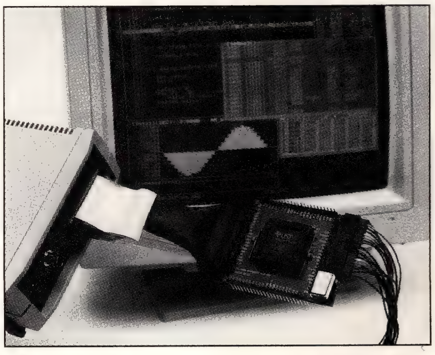
TMS320C5X ICE provides trace, overlay memory, and hardware breakpoints

In a world moving toward on-chip emulation, the TMS320C50 in-circuit emulator (ICE) stands out. Instead of using the debugging features built into the chip, the ICE reverts to removing the DSP on the target and replacing it with an emulation plug. In doing so, it provides features that aren't available with JTAG-based on-chip emulation.

The TMS320C5X provides on-chip emulation, which is accessible through a JTAG port on the chip. Although on-chip emulation provides an inexpensive method of debugging code, it cannot provide some useful features, including a 4-kword real-time trace, 64k×16-bit program-overlay memory, 64k×16-bit data-overlay memory, multiple hardware breakpoints, an event sequencer, a 16-channel external trace buffer, and a 16-bit external event trigger. The device emulates the TMS320C50 DSPs at clock speeds up to 57 MHz.

A DOS-based high-level debugger gives you up to 14 windows to view the operation of the DSP. It also includes graphical windows for displaying data. It is compatible with Texas Instruments' C compiler, assembler, and linker. A Windows version of the debugger ($995) is optional. The emulator costs $8995.—**David Shear**

Macrochip Research Inc, Carrollton, TX. (214) 242-0450. **Circle No. 498**



This in-circuit emulator does not use the on-chip emulation provided by the DSP chip.

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AK2354	●	●	●	●	●	1.9～5.5	1200 bps MSK MODEM
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CIRCLE NO. 103

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EMBEDDED SYSTEMS

DSP development software comes with hardware. The Hypersignal-Macro and Hypersignal-Acoustic DSP software-development package is now available with support for the National Instruments AT-DSP2200 PC plug-in board. The package also works with DSPower, a Windows-based package that allows users to develop DSP-based applications in a graphical environment. $3495 for hardware and software; $4195 with DSPower. **Signalogic**, Dallas, TX. (214) 343-0069.
Circle No. 456

Windows-based fuzzy-logic development tool. The TILShell 3.0 graphical development tool for creating fuzzy-logic-based applications includes C- and microcontroller-code generation. It comes in professional and standard editions. From $795. **Togai InfraLogic Inc**, Irvine, CA. (714) 975-8522.
Circle No. 457

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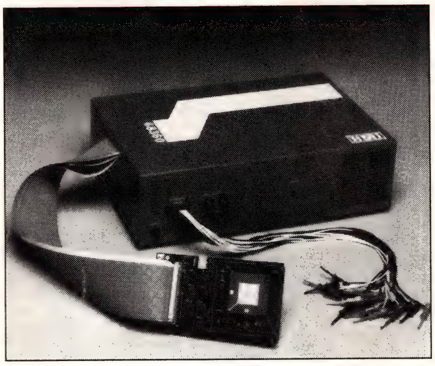

68360 ICE includes source-level debugger. The HMI-200 series in-circuit emulators (ICEs) support the Motorola 68360 µP and operate as fast as 25 MHz. The series includes two 16k×120-bit trace buffers, 256 kbytes of shadow RAM, and 256 kbytes of overlay RAM (expandable to 2 Mbytes). The trace buffer includes 16 external probes. The ICE provides the SourceGate II control and source-level debugging software, which runs on workstations and PCs. $16,000. **Huntsville Microsystems Inc**, Huntsville, AL. (205) 881-6005.
Circle No. 458

Z8 ICE works with PC. The ET-iCZ8 in-circuit emulator (ICE) for the Zilog Z8 handles devices running as fast as 16 MHz. Controlled by a PC, the device comes with a 40-pin DIP socket connector and a processor-specific probe to connect to the target. The device includes a 32-kbyte overlay RAM that can be mapped in 2, 4, 8, 16, or 32 kbytes. The device also provides a source-level debugger, an editor, and a project-management tool. From $2262. **Emulation Technology Inc**, Santa Clara, CA. (408) 982-0660.
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Simulate DSP16XX to gate level with DSP development system. The COSSAP DSP16xx design kit allows you to develop DSP-based applications with the AT&T DSP16xx DSP chips. A model developed by AT&T allows you to simulate the DSP16xx at a system level with your application software. The COSSAP VHDL simulator interface permits simulation to the gate level. The kit also includes AT&T software-development tools. $7500. **Cadis Software Ltd**, San Francisco, CA. (415) 615-7789.
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CIRCLE NO. 105

EMBEDDED SYSTEMS

Developer's kit gets you running on C40 DSP chip. The C40 developer's kit includes most of what you need to get started developing with the Texas Instruments' TMS320C40 DSP chip. It includes a DSP board for PCs, an optimizing C compiler, a source-level debugger, the Tartan FasTar math library, the Ariel DSP Expert library, and utilities. $5995; $4995 for universities. **Ariel Corp**, Highland Park, NJ. (908) 249-2900. **Circle No. 460**

Real-time debugger runs in X-Window environment. The MWX-ICE debugger, based on Microtec Research Inc's Xray debugger, now includes functions to control in-circuit emulators. The debugger runs stand-alone or connected to the Xray MasterWorks environment. It also supports the Motorola 68000 family and the Intel 80960CA/CF μP. $3000. **Applied Microsystems Corp**, Redmond, WA. (206) 882-2000. **Circle No. 461**

68306 development tool. The 8800 emulator/analyzer now supports the Motorola 68306 μP. It has 128-kbyte emulation memory and 16-kbyte trace buffer. Options are available for up to 64-kbyte trace and 2-Mbyte emulation memory. A clip-on emulation option allows you to connect the device directly to surface-mounted devices. From $10,500. **Orion Instruments Inc**, Menlo Park, CA. (415) 327-8800. **Circle No. 462**

Low-cost 68360 evaluation board. The SBC360 evaluation board for the Motorola 68360 μP includes 2 Mbytes of DRAM, 256 kbytes of SRAM, and 128 kbytes of flash EEPROM. Users can add as much as 16 Mbytes of DRAM via SIM connectors. The device provides all the external signals of the 68360. $895; $1995 with a BDM emulator and source-level debugger. **Embedded Support Tools Corp**, Canton, MA. (617) 828-5588. **Circle No. 463**

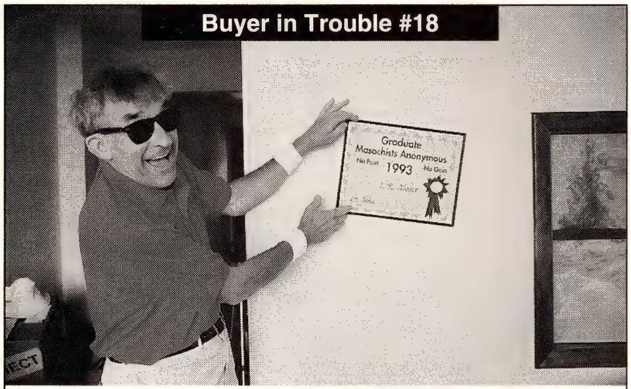
Program and erase a PIC16C71/C84 connected to a target. The TrueFlight programmer/downloader lets users program and erase a Microchip Technology PIC16C71 or PIC16C84 μC connected to a μC socket on the target. The device has a short cable that plugs into the μC socket on the target. Users can program and erase the μC on the TrueFlight board. Users can erase the EPROM-based PIC16C71 with an onboard UV source. $349. **Parallax Inc**, Rocklin, CA. (916) 624-8333. **Circle No. 464**

SHORTS

Xray/MTD multitasking debugger works with systems based on the C Executive real-time kernel. **JMI Software Systems Inc**, (215) 628-0840. **Circle No. 465**

STREAMS are now available for the Nucleus real-time operating system. **Accelerated Technology Inc**, (205) 661-5770. **Circle No. 466**

The LynxOS real-time operating system runs on the Motorola MVME162 68040-based VME board. **Lynx Real-Time Systems Inc**, (408) 354-7700. **Circle No. 467**



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12-bit ADCs speed up to 30 Msamples/sec

Achieving both high speed and high resolution is a challenging goal for the designers of ADCs. Currently, 14- and 16-bit devices don't have sampling rates much higher than 5 Msamples/sec (see "High-speed, high-resolution ADCs," EDN, October 28, 1993, pg 76). However, you can now find 12-bit converters with speeds of 30 Msamples/sec.

Comlinear Corp's CLC937 and CLC938 feature sampling rates of 25.6 and 30 Msamples/sec, respectively. These two ADCs round out the company's family of pin-compatible, high-performance 12-bit devices that also includes 15- and 20-Msample/sec parts. This family targets both frequency- and time-domain applications in IF sampling, communications, radar, IR and medical imaging, and instrumentation.

Spurious-free dynamic range, a key frequency-domain specification, of the CLC937 is 80.2 dB at 402 kHz and 67.1 dB at 4.986 MHz. In the time domain, the CLC938 operates with a maximum differential nonlinearity of 0.7 LSB and a S/N ratio (not including harmonics) of 56 dB at 95 MHz.

The wide analog input frequency range of the ADCs allows them to digitize IF signals directly. The CLC938's S/N ratio is 60 dB with analog inputs out to 50 MHz. Intermodulation distortion is typically 70 dB for the 937 and 75 dB for the 938.

These 2-pass subranging converters each include a broadband, 150-MHz input amplifier, a T/H amplifier, a reference, timing generators, error-correction circuitry, and an output latch/buffer. An external convert clock, analog input, and ±5 and ±15V power supplies are all that's required for operation. The company laser-trims gain and offset errors to assure accurate unit-to-unit matching. The company also guarantees no missing codes for both ADCs. The ADCs' nominal power dissipation is 6.9W, and they have an analog input range of 2V p-p.

Both commercial and military temperature-range versions are available in 2.28-in.-square, 40-pin packages. The 0 to 70°C ADCs cost $498 (100) and $687 (one to four pieces). The –55 to +125°C versions cost $1490 (100).—**Anne Watson Swager**

Comlinear Corp, Fort Collins, CO. (303) 226-0500. **Circle No. 453**

0.6-μm gate array targets system control

The art of designing custom or mother boards is in creating the system controls—the collection of glue logic, special controllers, and clocking subsystem—that make a system work. If you're casting about for an ASIC solution, look to the Motorola H4CPlus CMOS gate-array family. These arrays combine high gate densities with high pin counts and high-speed operation; they also feature single or dual 3 or 5V operation.

Gate densities range out to 178,000 usable gates, with internal clock rates up to 400 MHz. The gate arrays pump data at rates to 400 MHz using Current Mode Transceiver Logic (CMTL) with differential pairs, or to 200 MHz for single lines with active terminations. I/O macros also include PECL (pseudo ECL) and Gunning Transceiver Logic (GTL) for high-speed I/O. You can use the gate arrays as cache controllers or even to serve as small, high-speed caches for fast CPUs. Chip macros include PCI-bus-compliant buffers, including a 64-bit extension, and JTAG boundary scan for test. A single I/O cell can drive up to 24 mA; later releases will enable you to parallel two cells for a 48-mA drive.

Using a digital PLL macro, you can create clocks up to 75 MHz; using an analog PLL macro (provisions for two on-chip corners), clock rates can top 125 MHz. Rates can easily handle standard μPs such as the Pentium that run with a 66-MHz CPU clock.

- Extension of H4C gate-array family
- 0.6-μm L_{eff}, channelless, 3-layer metal
- To drive external clocks: 2 analog PLLs (125-MHz, 250-psec jitter) or digital PLLs (75-MHz, 500-psec jitter)
- 28,400 to 178,000 available gates
- 2-input NAND gate delay (2 loads)=280/420 psec at 5/3V
- Current Mode Transceiver Logic (CMTL) for fast I/Os, buses 200/400 MHz (differential), also PECL, GTL
- 128 to 313 package pins
- OMPAC (ball grid array), PQFP, and MicroCool (QFP with heat sink) packages
- JTAG boundary scan built into I/O macros
- 3, 5V operation (1 or mixed)

H4CPlus arrays rely on a self-aligned, twin-tub process with short n-channel transistors to reduce feature size and power dissipation. Typical power dissipation is 1 μW/gate at 3.3V and 3 μW/gate at 5V (0.05-pF load). Array packaging includes PQFPs, MicroCool (QFP with a heat sink), and OMPAC (OverMolded Pad Array Carrier). OMPAC combines a ball-grid-array interconnect to the system board with a small, double-metal pc board that holds the chip. I/O pads are conventionally bonded to the board, which routes the signals to the underlying ball grid array. An OMPAC package is smaller than an equivalent PQFP. OMPACs are 51 and 26% smaller than 160- and 208-pin PQFPs. The ball grid array reduces connection inductance and opens up pitch between pins for easier signal routing; it is also self-aligning.

The Macrocell library includes 1-, 2-, and 4-port asynchronous SRAMs. The design environment uses Motorola, Cadence, and Mentor Graphics tool sets, as well as individual point tools, such as Synopsys synthesis compilers. —**Ray Weiss**

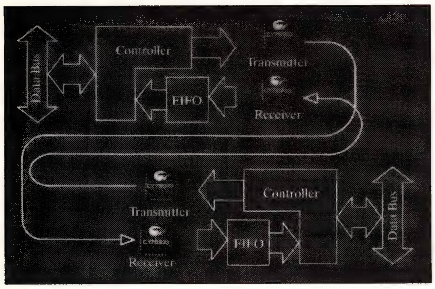
Motorola Inc, ASIC Div, Chandler, AZ. (602) 814-4124. **Circle No. 454**

H4CPlus CMOS gate arrays

Array	Available gates	Die size	Die pads	I/O cells	Package pins
H4CP028*	28,400	239	176	160	128 to 169
H4CP048	48,100	287	216	208	128 to 225
H4CP075	74,520	337	256	256	128 to 225
H4CP0109*	109,368	391	304	312	160 to 208
H4CP0146*	145,544	438	344	360	160 to 313
H4CP028	178,000	476	376	400	160 to 313

*Available in second phase

INTEGRATED CIRCUITS



Serial chip set communicates at 330 Mbps. The HOTLink (high-speed optical transceiver link) chip set comprises a transmitter (CY7B923) and a receiver (CY7B933) that translate between 8-bit parallel and serial data forms, handling serial data rates as great as 330 Mbps. The serial data can be unencoded or use 8B/10B coding for compatibility with Fibre Channel. The set needs no external components for clock and timing recovery and has a self-test capability. $60 (100). **Cypress Semiconductor**, San Jose, CA. (408) 943-2600. **Circle No. 420**

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RAMDAC offers Advanced Feature Connector. The Px2085 MediaDAC offers 24-bit color performance and a VESA Advanced Feature Connector interface to speed the merger of video and graphical display data. It also offers color-space conversion, interpolated zooming, and separate contrast and brightness controls for video windows. Pixel clocks run to 85 MHz for 24-bit color and 135 MHz for 5:6:5 color. $50 (1000). **Cirrus Logic**, Fremont, CA. (214) 985-2340. **Circle No. 421**

Graphics ICs include VL and PCI local-bus interfaces. These graphical-user-interface-accelerator graphics ICs have local-bus interfaces. The CL-GD5430 ($30 (1000)) offers 32-bit interfaces and works with 1- and 2-Mbyte frame buffers. The CL-GD5429 ($27) has a VL-bus interface and features a true-color RAMDAC. The 64-bit CL-GD5452/3 ($65) uses video-RAM buffers and provides true-color displays at resolutions up to 1280×1024 pixels. The 2-chip set also includes a palette DAC with video overlay and color-key support. **Cirrus Logic**, Fremont, CA. (510) 226-2123. **Circle No. 423**

Flash comes in 4-Mbit, 5V version. The Am29F040 is a 4-Mbit flash memory with sector-erase capability that operates with a single 5V supply. It allows OEMs to protect specific 64-kbyte sectors against erasure in embedded applications. The device has self-completing program and erase commands and can suspend and resume an erase operation to allow reading data from another sector without waiting for erasure to finish. Devices come in 90-, 120-, and 150-nsec speed grades in PLCC, TSOP, PDIP, and other packages. A 90-nsec version, from $34.20 (1000). **Advanced Micro Devices**, Sunnyvale, CA. (408) 749-5703. **Circle No. 424**

ATM chips support WAN needs. Supporting seven data rates from 34 to 155 Mbps, the Bt8220 transceiver handles all ATM physical-layer functions. A companion chip, the Bt8215, serves as a bidirectional cell buffer. The Bt8215

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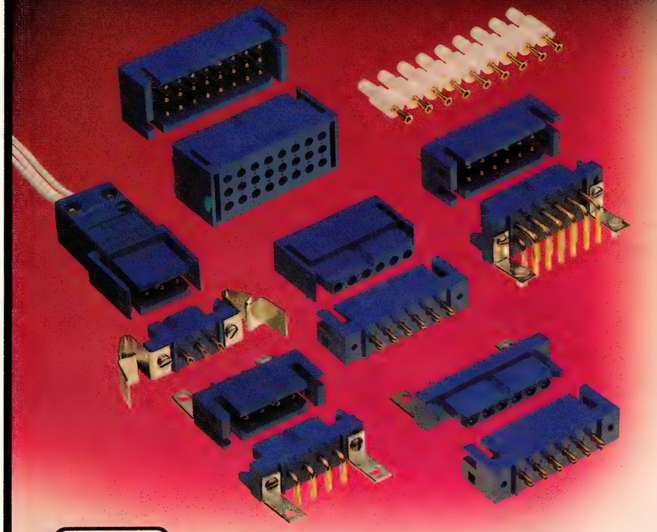

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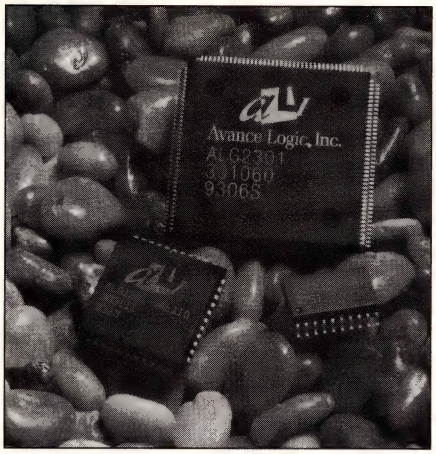
CIRCLE NO. 27

handles data as ATM cells, automatically maintaining word alignment when formatting data between its 8- and 32-bit ports. It also works with HDLC and SMDS packets. $90 for the Bt8215; $85 for the Bt8220. (1000) **Brooktree Corp**, San Diego, CA. (619) 452-7580. **Circle No. 425**

IGBT controls 45 kW. The IXSK 50N60AU1 comprises a short-circuit-rated IGBT (10-µsec short-circuit withstand time) and a 35-nsec ultrafast-recovery diode mounted in a TO-264 package. The device has a rated blocking voltage of 600V and collector current of 74A. Maximum saturation voltage is 2.7V with a typical fast-fall time of 200 nsec. $14.38 (1000). **IXYS Corp**, Santa Clara, CA. (408) 982-0700. **Circle No. 426**



PCI chip set makes i486 graphics affordable. The ALG2301 chip set comprises a 24-bit RAMDAC, a dual programmable dot clock, and a graphics-accelerator chip. The 32-bit graphics accelerator complies with Revision 2.0 of the peripheral-component-interconnect (PCI) specification. The chip supports zero-wait-state burst-mode and autoconfiguration features. It connects directly to the PCI bus without any glue logic. The chip set is compatible with EPA Energy Green Star requirements and supports resolutions as high as 1280×1024 pixels. The RAMDAC supports 16.7 million colors and operates at 110 MHz. $20 (OEM). **Avance Logic Inc**, Fremont, CA. (510) 226-9555. **Circle No. 427**

ADC performs full Nyquist sampling. The SP674B ADC includes a 12-bit successive-approximation ADC with 3-state output latches, an internal reference, a clock, and a S/H amplifier. Features include a total harmonic distortion of –80 dB, a spurious-free dynamic range of 85 dB, an S/N plus distortion of 72 dB, and a S/N ratio of 72.5 dB, all measured at the Nyquist input frequency of one-half the IC's 67-kHz sampling rate. $9 (1000). **Sipex Corp**, Billerica, MA. (508) 671-1940. **Circle No. 428**

16-channel DAC comes in 52-pin package. The MP7642 features 16 independent, 2-quadrant multiplying, 8-bit DACs, and a power consumption of 325 mW. The IC also includes a serial digital input-data-address port plus an internal chip-address decoder. Digital-word to V_{OUT} settling time to 8 bits is 750 nsec, and the device has a 1-MHz-reference input bandwidth. In PQFP, $17.48. **Micro Power Systems**, Santa Clara, CA. (408) 727-5350. **Circle No. 429**

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CIRCLE NO. 28

Handheld LCD DMM/DSOs display transient waveform anomalies

Look out, Fluke, Leader Instruments, and HC Protek! There's a large vehicle looming in your rearview mirror, and it's moving fast. The license plate is from Oregon, and the name on the side is Tektronix. Onboard is a new product line—one that users are bound to compare with some of the hottest selling measurement products: handheld, battery-powered DMM/digital storage oscilloscopes (DSOs) with LCDs. To emphasize that the items, priced from $859, are DMMs first and DSOs second, Tek calls them Tek*Meters*.

The $859 THM 550, with its single DSO channel, includes one of the custom ICs. The $999 THM 560 and $1259 THM 565—both of which offer two DSO channels—include two of the chips. (The THM 565 has a backlit display and more features than the other two models.) When you power up one of the units, it behaves as a 4000-count true-rms DMM that offers such functions as resistance measurement to 40 MΩ, an audible continuity indication, and a diode-check mode. Pushing one button turns on the DSO function. The DSO bandwidth is 5 MHz; each DSO channel can acquire 25 Msamples/sec in real time. The 2-channel models sample simultaneously.

Pushing a single button changes TekMeters' 6-in. (diagonal) LCDs from 4000-count numeric displays in the DMM mode to 1- or 2-channel, 5-MHz-bandwidth waveform displays in the real-time-sampling DSO mode.

Six alkaline AA cells power the units for four hours. You can also use rechargeable cells. With batteries, the 8.5×5.5×1.6-in. units weigh 2.2 lb. Accessories include an ac-powered RS-232C adapter that replaces the batteries and does not defeat the isolation between the inputs and the case. Across their inputs, the products withstand 6-kV surges and 850V dc or 600V rms continuously.— **Dan Strassberg**

Tektronix Inc, Beaverton, OR. (800) 426-2200. **Circle No. 444**

Power analyzer measures fluctuating harmonics. The PM3000A makes all IEC555 harmonic measurements as well as flicker measurements specified in IEC868. The instrument displays results as real-time bar graphs, charts of harmonics vs time, or tables. Printouts can contain pass/fail indicators. The unit operates over the standards' full range and requires no calibration checking or range switching. $11,900. **Voltech Inc**, Ashland, MA. (508) 881-7329. **Circle No. 445**

"Executable front panels" come with VXI Bus instruments. This front-panel graphical-user-interface software comes with the vendor's VXI Bus instruments. The software eases the problems users have in performing operations with VXI Bus instruments, which require software, that pose no difficulties with conventional front-panel-controlled instruments. The software comes on a 3.5-in. floppy disk and does not increase the price of the equipment. **Racal Instruments**, Irvine, CA. (800) 722-3262. **Circle No. 446**

Analog measurement technique finds open circuits. Opens Express locates open circuits to the device pin on surface-mount pc boards. It also identifies misaligned parts. The technique works by applying an ac voltage to each device lead and using a plate above the pc board to measure the voltage coupled to the IC package. There is an order-of-magnitude difference between the voltage coupled through an open circuit and that coupled through a proper connection. The open-circuit detector is a $10,000 option for the vendor's GR228X board-test systems equipped with the analog fault-test module (AFTM). The option costs $20,000 on systems not equipped with AFTM. **GenRad Inc**, Concord, MA. (508) 369-4400. **Circle No. 447**

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$99 device measures resistance, ac voltage, and ac current. Model 30 clamp-on digital meter, which measures to 400A and 600V ac, conforms to IEC 1010. UL, CSA, and TUV certification are pending. The unit, which receives power from a 9V battery, is accurate within 1.3% for 1 year after calibration. **Fluke Corp**, Everett, WA. (800) 873-5853. **Circle No. 448**

SCSI test system makes DMA transfers at 6.25 Mbps. The Spirit I SCSI-device-test system uses a RISC-based interface and assembly-language software to obtain sustained synchronous speeds of 6.25 Mbps. The system supports three testing modes: interactive with an integrated exerciser, automated batch testing under the control of ASCII files, and direct access to the SCSI bus via the user's programs. You can configure the interactive mode to support 50 SCSI commands. $1995. **Spectre Engineering Inc**, Berkley, MI. (313) 547-2098. **Circle No. 449**

Programmable video generator offers dot-clock rates to 120 MHz. The Astro VG-812 works with monitors that have resolutions as high as 1280×1024 pixels, horizontal scanning frequencies to 130 kHz, and frame rates to 150 Hz. The unit, which stores as many as 40 combinations of timing setups and patterns in an EEPROM, offers full control of the horizontal and vertical sync signals. $3500. **Team Systems Inc**, Santa Clara, CA. (408) 720-8877. **Circle No. 450**

Test 10-Mbps wide area networks. The Model 77 handheld tester tests synchronous and asynchronous wide-area networks from 10 bps to 10 Mbps. It accepts 13 plug-in interface modules from RS-232C to fractional T1 with data and VF drop and insert. The unit produces pseudorandom bit sequences from 63 bits to 8 Mbits long. Prices for the ac-powered tester begin at $340. **International Data Sciences Inc**, Warwick, RI. (401) 737-9900. **Circle No. 451**

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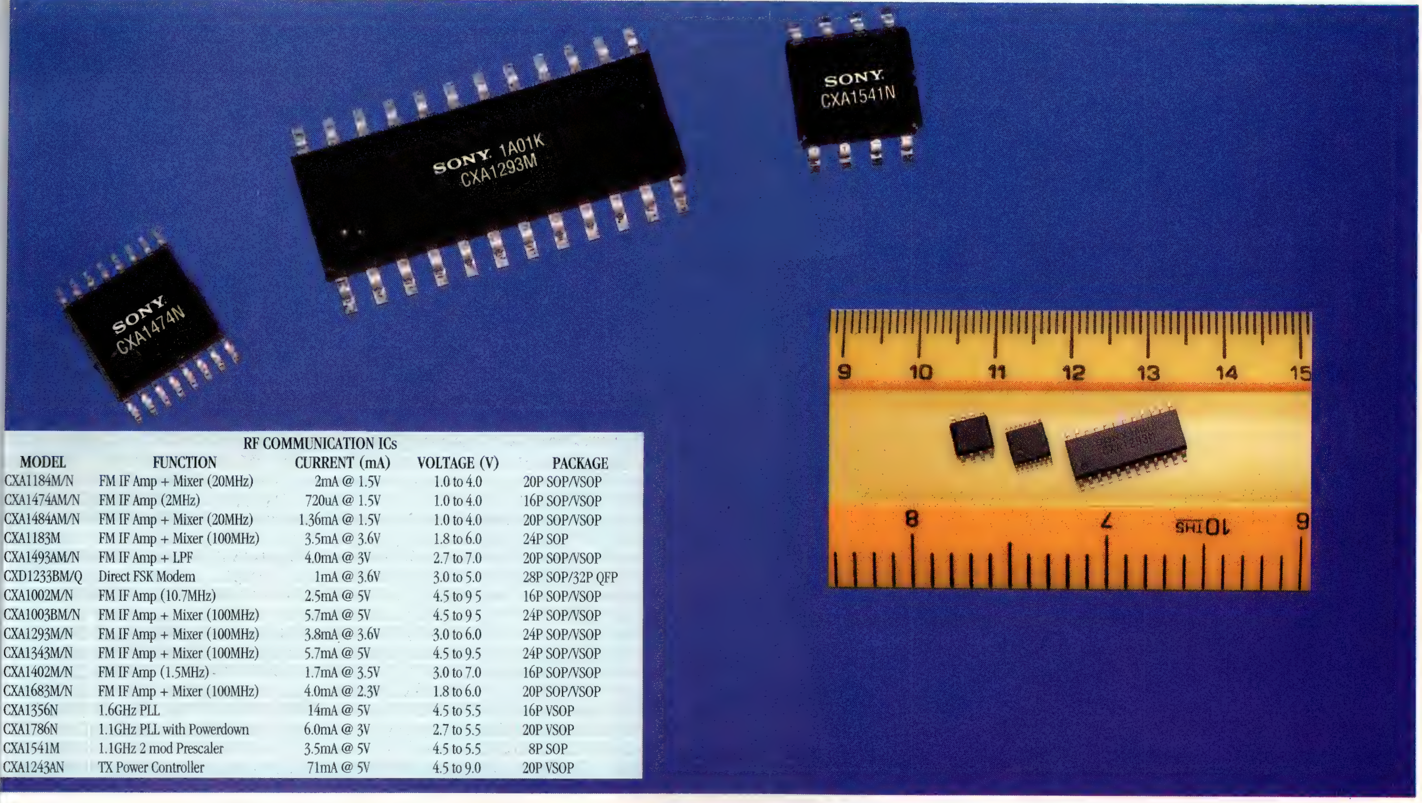

RF COMMUNICATION ICs

MODEL	FUNCTION	CURRENT (mA)	VOLTAGE (V)	PACKAGE
CXA1184M/N	FM IF Amp + Mixer (20MHz)	2mA @ 1.5V	1.0 to 4.0	20P SOP/VSOP
CXA1474AM/N	FM IF Amp (2MHz)	720uA @ 1.5V	1.0 to 4.0	16P SOP/VSOP
CXA1484AM/N	FM IF Amp + Mixer (20MHz)	1.36mA @ 1.5V	1.0 to 4.0	20P SOP/VSOP
CXA1183M	FM IF Amp + Mixer (100MHz)	3.5mA @ 3.6V	1.8 to 6.0	24P SOP
CXA1493AM/N	FM IF Amp + LPF	4.0mA @ 3V	2.7 to 7.0	20P SOP/VSOP
CXD1233BM/Q	Direct FSK Modem	1mA @ 3.6V	3.0 to 5.0	28P SOP/32P QFP
CXA1002M/N	FM IF Amp (10.7MHz)	2.5mA @ 5V	4.5 to 9 5	16P SOP/VSOP
CXA1003BM/N	FM IF Amp + Mixer (100MHz)	5.7mA @ 5V	4.5 to 9 5	24P SOP/VSOP
CXA1293M/N	FM IF Amp + Mixer (100MHz)	3.8mA @ 3.6V	3.0 to 6.0	24P SOP/VSOP
CXA1343M/N	FM IF Amp + Mixer (100MHz)	5.7mA @ 5V	4.5 to 9.5	24P SOP/VSOP
CXA1402M/N	FM IF Amp (1.5MHz)	1.7mA @ 3.5V	3.0 to 7.0	16P SOP/VSOP
CXA1683M/N	FM IF Amp + Mixer (100MHz)	4.0mA @ 2.3V	1.8 to 6.0	20P SOP/VSOP
CXA1356N	1.6GHz PLL	14mA @ 5V	4.5 to 5.5	16P VSOP
CXA1786N	1.1GHz PLL with Powerdown	6.0mA @ 3V	2.7 to 5.5	20P VSOP
CXA1541M	1.1GHz 2 mod Prescaler	3.5mA @ 5V	4.5 to 5.5	8P SOP
CXA1243AN	TX Power Controller	71mA @ 5V	4.5 to 9.0	20P VSOP

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CIRCLE NO. 109

Mixed-signal design tool adds programmable logic

Using one tool, you now can design and simulate a system that includes programmable logic and discrete digital and analog parts. PLSyn, a new member of Microsim's Design Center family, adds the programmable-logic capability. You can describe the programmable-logic design directly on the schematic (along with other analog and digital devices); use a synthesis language or logic symbols; or combine both methods. The software accommodates hierarchical designs with tens of thousands of gates.

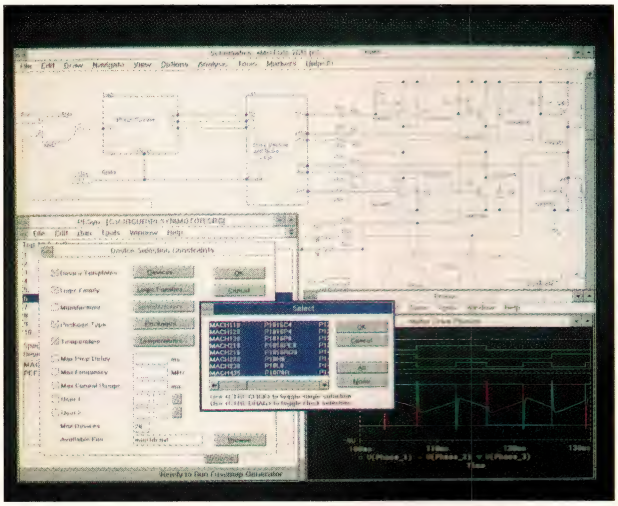
PLSyn lets you simulate designs, before and after physically implementing the programmable logic, using either timing estimates or timing data from the actual device implementation. You can run the simulation on either PLogic (for completely digital designs) or on PSpice A/D (for mixed analog/digital designs). The Design Center's integrated environment provides interactive stimulus editing and graphical waveform analysis.

Once your programmable-logic design is complete, PLSyn selects the most desirable PLD from a library of more than 4000; you can base a decision on constraints such as price, speed, and power consumption. The software automatically partitions the design to fit into one or more PLDs—or even different types of PLDs.

PLSyn will be available in March. Design Center with PLSyn costs $3500 to $5500 ($4550 to $7150 internationally) for use on PCs under Microsoft Windows, and $7600 to $14,500 ($9900 to $18,850 internationally) for use on Sun workstations under Open Windows. A discount of 25% is available until May.—**Doug Conner**

MicroSim, Irvine, CA. (714) 770-3022.

Circle No. 477



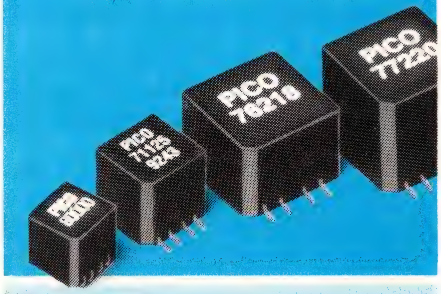
PLSyn extends the mixed-signal design capabilities of Design Center to handle programmable logic.

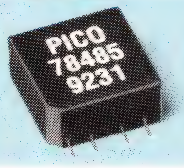
Tool helps identify critical system parts

When analyzing system performance, you often look for sensitivity to changes in component parameters. Complex systems may include electrical, mechanical, hydraulic, and other component types. The Critical Part Identifier (CPI) option to the Saber mixed-signal simulator computes sensitivity of all system parts, so you easily see which parts have the greatest effect on system performance. In addition, the tool determines which components exceed safe operating conditions. A report generator summarizes results. CPI is a $7000 option to Saber.—**Doug Conner**

Analogy, Beaverton, OR. (503) 626-9700.

Circle No. 478





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CIRCLE NO. 30

ELECTRONIC DESIGN AUTOMATION

VHDL simulators run under Unix. ViewSim/VHDL combines gate-level and VHDL simulation for ASIC and system design. ViewSim/VHDL costs $31,000. View/VHDL offers VHDL-only simulation and costs $18,500. Both products run under Unix and are available now. **Viewlogic Systems Inc**, Marlboro, MA. (508) 480-0881. **Circle No. 480**

Run mixed analog and digital simulations under Windows. Using Simbus for Windows you can co-simulate analog and digital circuits using Viewlogic's ViewSpice and Viewsim Tools. Simbus runs under the company's Workview Plus design environment and costs $4000. A simulator-specific integration package, which is required, costs $2000 for ViewSpice. ViewSpice is a new analog simulator based on Berkeley Spice 3F2. The simulator retains compatibility with Spice 2G6. The Unix-based Powerview version costs $7500, and the version that runs under Microsoft Windows costs $3500. An 8000-part model library is optional. **Viewlogic Systems Inc**, Marlboro, MA. (508) 480-0881. **Circle No. 481**

Accelerate implementation of DSP designs. This interface to Comdisco Systems' Signal Processing WorkSystem (SPW) lets users design, simulate, and optimize a DSP system-level design and then transfer the design to Compass's Datapath Synthesizer and Datapath Compiler tools to create an ASIC design. The DSP Design Option costs $20,000 and is available now. **Compass Design Automation**, San Jose, CA. (408) 433-4880. **Circle No. 482**

Use Lsim and QuickSim II models in Verilog simulations. The Lsim-VCI (Verilog Cosimulation Interface) lets you use IC designs created with Lsim in Verilog hardware-description-language simulations. Lsim provides detailed modeling of analog and digital designs. Lsim-VCI costs $19,500. You can also use QuickSim II models in a Verilog simulation using QuickSim-II VCI, which costs $19,500 and is available now. **Mentor Graphics**, Wilsonville, OR. (503) 685-7000. **Circle No. 483**

Component information system helps aerospace and defense contractors identify potential supply problems. This component-information system (CIS) has modules developed by Hughes Aircraft Co. CIS helps you maintain designs that may remain in service for 20 years or more. The system includes automatic warning reports, sending warnings by electronic mail to designated managers when a part is approaching obsolescence or when a supplier will no longer be manufacturing a part. You can stockpile, find a substitute, or otherwise prepare for the part-supply problem. The CIS with the Hughes modules starts at $100,000. **Aspect Development Inc**, Los Altos, CA. (415) 941-2525. **Circle No. 484**

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Module generator improves synthesized-FPGA data-path designs. The module-generation feature of the Core logic-synthesis tool provides a path from structured logic in VHDL or Verilog hardware-description language through logic synthesis to a technology-specific netlist and place-and-route tools. The software implements arithmetic and relational operators for 2- tp 64-bit designs. Multiple implementations provide area and delay tradeoffs. The software costs $5000 to $8000 for DOS systems and $15,000 to $30,000 for Unix systems. **Exemplar Logic**, Berkeley, CA. (510) 849-0937. **Circle No. 485**

Low-cost FPGA-design starter kit. Four design kits for FPGAs are available. The $695 Integrator Series FPGA starter kit includes the TI-ALS action logic system with Viewlogic or OrCAD libraries and utilities, the Module Mover, and logic-integration software. The high-end design kit, the FPGA deluxe, costs $4495 and includes schematic capture, PLD-equation entry, simulation, logic synthesis, and a device programmer. **Texas Instruments**, Dallas, TX. (800) 477-8924, ext 4500. **Circle No. 486**

Design software runs on Macs. The Run EDS software package provides schematic capture, pc-board layout, and analog and digital simulation for Macintosh computers. The integrated program provides schematic capture through multilayer pc-board layout and simulation. The software provides forward and back annotation and cross-highlighting of schematic and pc-board layout. Prices range from $975 for schematic capture to $20,500 for a complete Run EDS system including mixed analog-digital simulation. **MicroCad Partners**, Burnsville, MN. (612) 895-8236. **Circle No 487.**

Software automates creation of ASIC test programs. ViewTest comprises a set of sequential test tools based on Sunrise Test Systems Inc, a Viewlogic strategic partner. Viewlogic claims the software improves design testability, shortens the design time of ASICs, increases product quality, and decreases test costs. The company has fully integrated ViewTest into the Powerview Unix-based work environment. Price starts at $75,000 for a complete system. **Viewlogic Systems Inc**, Marlboro, MA. (508) 480-0881. **Circle No. 488**

FPGA-design software extends capabilities. AT&T's Orca Development System (ODS) 2.0 software extends the features of the previous version and supports the company's new 12,000- and 15,000-usable-gate FPGAs (2Cxx family). The features include back-annotated timing for postrouting simulation to an original schematic, netlist merge, algorithm improvements for data-path-intensive designs, and a design editor with incremental logic-change capability. Beta versions of ODS 2.0 are available now, and production is scheduled for February. The PC version costs $4500, and the Sun version is $7500. **AT&T Microelectronics**, Allentown, PA. (800) 553-2448, ext 896. **Circle No. 489**

SHORTS

Texas Instruments and Mentor Graphics have announced a high-density interconnect (HDI) multichip-module (MCM) design kit for Mentor Graphics' MCM Station. **Mentor Graphics**, (503) 685-7000. **Circle No. 490**

Check Verilog HDL designs for syntax and semantic errors before simulation and synthesis using Verilint. The software runs on Sun, HP, and DEC Alpha workstations and costs $2000. **InterHDL**, (408) 749-8775. **Circle No. 491**

Chronologic Simulation upgrades Verilog-XL licenses to VCS 2.0 for $1000 until January 31, 1994. Limited to one upgrade license per customer. **Chronologic Simulation**, (415) 965-3312. **Circle No. 492**

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**3.94″x6.3″. The metric dimension is exact.*

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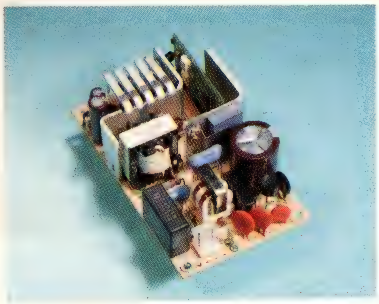
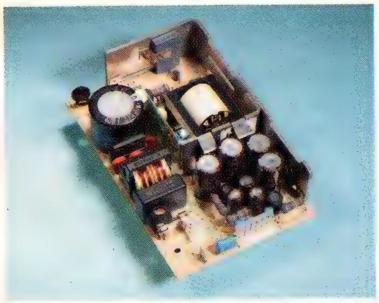


3″x5″ Footprint 40W
Model KRW 352KV



3.94″x6.3″ Footprint 65W
Model MRW 171KV

MODEL	POWER Watts	OUTPUT #1 Volts	Amps	OUTPUT #2 Volts	Amps	OUPTPUT #3 Volts	Amps
KRW 350KV	40	+5	0.5-3.0 (typ) (4.0 max)	+12	0.3-2.0 (typ) (3.0 max)	−12	0-0.1 (typ) (0.3 max)
KRW 351KV	40	+5	0.5-3.0 (typ) (4.0 max)	+15	0.3-1.6 (typ) (2.0 max)	−15	0-0.1 (typ) (0.3 max)
KRW 352KV	40	+3.3	0.5-3.0 (typ) (4.0 max)	+12	0.3-2.0 (typ) (3.0 max)	−12	0-0.1 (typ) (0.3 max)
MRW 150KV	35	+5	1.0-2.2 (typ) (4.0 max)	+12	0.6-1.8 (typ) (2.5 max)	−12	0-0.1 (typ) (0.3 max)
MRW 151KV	35	+5	1.0-2.2 (typ) (4.0 max)	+15	0.6-1.4 (typ) (2.0 max)	−15	0-0.1 (typ) (0.3 max)
MRW 160KV	50	+5	1.0-5.0 (typ) (6.0 max)	+12	0.5-2.0 (typ) (2.5 max)	−12	0-0.1 (typ) (0.5 max)
MRW 161KV	50	+5	1.0-5.0 (typ) (6.0 max)	+15	0.5-1.5 (typ) (2.0 max)	−15	0-0.1 (typ) (0.4 max)
MRW 170KV	65	+5	0.8-5.0 (typ) (7.0 max)	+12	0.3-1.7 (typ) (2.5 max)	−12	0.3-1.7 (typ) (2.5 max)
MRW 171KV	65	+5	0.8-5.0 (typ) (7.0 max)	+15	0.3-1.3 (typ) (2.0 max)	−15	0.3-1.3 (typ) (2.0 max)

1 This KEPCO product is backed by a firm **1-YEAR WARRANTY**

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CIRCLE NO. 110

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SR770	***$6500***

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- GPIB interface, internal or external timebases

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CIRCLE NO. 111

COMPONENTS

Filter modules suit LAN applications. The PE-68501, PE-68502, and PE-68503 filter/magnetics modules for LAN applications implement a 100-Mbps TP-FDDI data link over data-grade, unshielded twisted-pair cable. The units serve as a cable interface for an MLT-3 transceiver. Each module includes transmit/receive filters to reduce ringing, overshoot, and noise problems. $2.52, $4.92, and $4.99 for the PE-68501, -68502, and -68503, respectively (1000). **Pulse Engineering Inc**, San Diego, CA. (619) 674-8100.
Circle No. 431

RC networks are surface-mountable. PRC207 RC networks operate at frequencies as high as 10^9 Hz. Resistance and capacitance values range from 15 to 200Ω and 10 to 200 pF, respectively. Standard tolerance equals ±20%, but ±5 and ±10% tolerances are available. Capacitor voltage ratings range from 250V for 10-pF units to 10V for 200-pF capacitors. Operating range spans –55 to +150°C. $0.20 (10,000). Delivery, six weeks ARO. **California Micro Devices Corp**, Milpitas, CA. (408) 263-3214.
Circle No. 432

Chips feature high capacitances. These additions to the MCS Series bring the capacitance value to as high as 6.8 μF. Use of thin-film bonding eliminates the cracking problems often found in large ceramic-chip capacitors. MCS32 units have values of 10,000 pF to 3.3 μF. Capacitance values for MCS43 and MCS53 devices range from 22,000 pF to 6.8 μF and 33,000 pF to 6.8 μF, respectively. $0.018 to $0.67 (10,000). Delivery, stock to 10 weeks ARO. **Rohm Corp**, Antioch, TN. (615) 641-2020.
Circle No. 433

Transformers are surface mountable. The SPT-043 and SPT-044 surface-mountable telephone-interconnect transformers for high-speed-data (V.32.bis) applications match 600Ω primary and secondary impedances at 0-dc loop currents. The -044 has a split primary and secondary winding. THD (measured at –10 dBm and 60 Hz) for both units is –74 dB typ. The units come in a 10-lead gull-wing package measuring 0.52×0.65×0.41 in. $3.52 and $4.01 (OEM qty) for the SPT-043 and SPT-044, respectively. Delivery, stock to six weeks ARO. **Prem Magnetics Inc**, McHenry, IL. (815) 385-2700.
Circle No. 434

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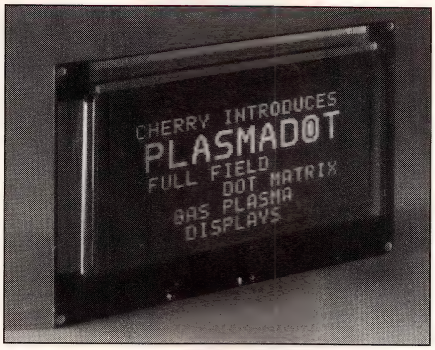

Displays have wide viewing angle. PD Series dot-matrix gas plasma displays feature flicker-free brightness and a 130° viewing angle. The PD02-D104 has 128×64 pixels and a 5.10×2.54-in. display area. The PD16-D862 is a 280×120-pixel model with an 8.38×4.54-in. viewing area. Both units feature an RS-232C interface. The full-field designs accommodate graphics and text. PD02-D104, $236.30; PD16-D862, $933.83. **Cherry Electrical Products**, Waukegan, IL. (708) 360-3434.
Circle No. 435

Filter provides interface. The 78Z041SM universal 10Base-T filter magnetic module provides the physical-layer interface between an RJ45 connector and a front-end transceiver. The module includes transmit and receive channels (each with a filter, isolation transformer, and common-mode choke) and meets IEEE 802.3 standards. The unit comes in a 16-pin surface-mount package. $2.50 to $2.60 (OEM qty). **FEE Fil-Mag**, San Diego, CA. (619) 569-6577.
Circle No. 436

Slide switches save space. MRC Series slide switches come in packages as small as 0.118×0.28×0.67 in. The devices are available in vertical and right-angle styles in single- or double-pole models with two, three, or four positions. Contacts are rated for 300 mA at 4V dc, and electrical life measures 5000 cycles min. $0.46 (1000) for the MRC12. **MORS/ASC**, Wakefield, MA. (617) 246-1007.
Circle No. 437

DPMs have adjustable offset. The DPM5130B 3-digit digital panel meter (DPM) features an adjustable zero offset for use with a variety of transducer and bridge circuits; a zero (000) display can be set while the input voltage or current level is above or below zero. Basic measuring range is –99 mV to +999 mV dc, and zero-adjustment range is –90 mV to +200 mV. You can extend the measuring range to –99 to +999V dc. $29.50. Delivery, stock to six weeks ARO. **DI International Inc**, Huntington, NY. (516) 673-6866.
Circle No. 438

PLCC sockets have low profile. PRO-200 plastic-leaded chip-carrier (PLCC) sockets have an above-board height of 0.185 in. max. Seven models cover PLCC configurations from 20 through 84 pins. Insulators are high-temperature, glass-filled PPS thermoplastic and carry a 94V-0 UL rating. Mating lifetime is 100 cycles. $1.88 (1000) for an 84-pin model. **Components Corp**, Denville, NJ. (201) 627-0290.
Circle No. 439

Magnetic sensors replace switches. OHB900 magnetic-sensor assemblies replace mechanical switches in applications requiring long life and high reliability. The units comprise a digital Hall-effect sensor and a rare-earth magnet in a plastic housing on opposite sides of an 0.125-in.-wide slot. The sensor switches output state when a ferrous object blocks the gap in the sensor. $3.33 (1000). **Optek Technology Inc**, Carrollton, TX. (214) 323-2200.
Circle No. 440

Power relays for high-density applications. G6D power relays measure 6.5×17.5×13.5 mm and require 45% less board space than comparable power models. The Form A contacts are rated to switch 5A at 250V ac or 30V dc. Power consumption equals 200 mW. With a 2A-at-250Vac/30Vdc load, the relays have a 300,000-operation lifetime. Sealed construction makes the unit compatible with water-soluble flux-immersion cleaning methods. $4.23. **Omron Electronics Inc**, Schaumburg, IL. (708) 843-7900.
Circle No. 441

Mixer operates to 1900 MHz. The RMS-11X broadband surface-mount mixer suits applications in the 5- to 1900-MHz range. The device resides in a 0.25×0.31×0.2-in. package and has a 1-dB compression at 1-dBm RF input and has a 6-dB conversion loss. All pads have solder over a nickel barrier for improved leach resistance. Operating range spans –55 to +100°C. **Mini-Circuits**, Brooklyn, NY. (718) 934-4500.
Circle No. 442

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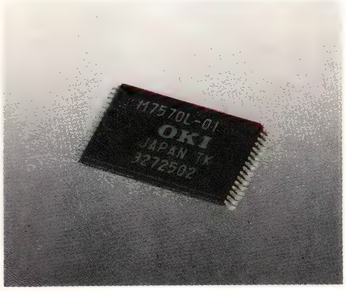

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Part No.	Supply voltage	Function				Status
		Companding law	PCM CODEC G.714	ADPCM CODEC G.721	Master clock freq.	
MSM7541/42	3.0-3.8V	7541/μ-law 7542/A-law	○		not needed	M.P
MSM7543/44	4.75-5.25	7543/μ-law 7544/A-law	○		not needed	M.P
MSM7570	4.5-5.5V	μ/A-law selectable	○	○	7570, 19.2/12.288MHz	M.P
MSM7570L/90L	2.7-3.6V	μ/A-law selectable	○	○	7590, 10.368MHz	M.P

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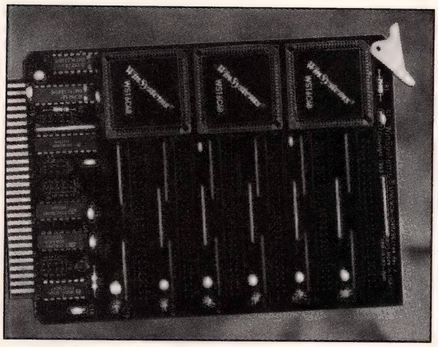
REED RELAY/REED SWITCHES OPTICAL MOS RELAYS LED PRINT HEADS MEMORIES MEMORY MODULES

CIRCLE NO. 113

BOARDS & BUSES



I/O card adds interrupts to STD. The LPM-IO144 brings 144 bidirectional I/O lines to a single STD card. You can program each line as input, output, or output with read-back. As many as 72 lines can generate an interrupt on an incoming transition. Output lines sink 12 mA. The board costs $350; 96- and 48-line versions are available for $295 and $240, respectively. **WinSystems Inc**, Arlington, TX. (817) 274-7553.
Circle No. 500

DSP board offers protocol conversion. The ASM-C/S DSP board uses the TMS320C31 DSP chip but offers interfaces compatible with the TMS320C40. The card serves as an accelerator for C31- or C40-based systems or functions as a stand-alone DSP with the addition of SRAM. It is available in half-size XT ($495) or 3U VME ($595) card sizes. **Sonitech International Inc**, Wellesley, MA. (617) 235-6824. **Circle No. 501**

I/O board links to DSP. Linking to the company's DSP boards via the DSP-Link bus, this 32-channel digital I/O board allows the DSPs to use the Arcom signal-conditioning bus. The board allows single- or double-buffered bidirectional data transfers and has onboard timers for generating sample rates as high as 200 kHz. $1045. **Spectrum Signal Processing**, Burnaby, BC, Canada. (604) 421-5422.
Circle No. 502

VME board handles 4-channel audio. The MMI-4211 VME board provides four independent DSP channels, each with a 16-bit ADC, a 16-bit DAC, a sample-rate generator, and analog I/O lines. The converters work with 8- to 48-kHz sample rates and can mix the outputs under program control. The $5950 board comes with the Dispatch audio-signal-processing software package. **Vigra Inc**, San Diego, CA. (619) 597-7080. **Circle No. 503**

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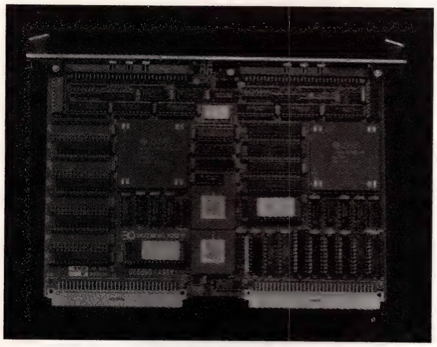
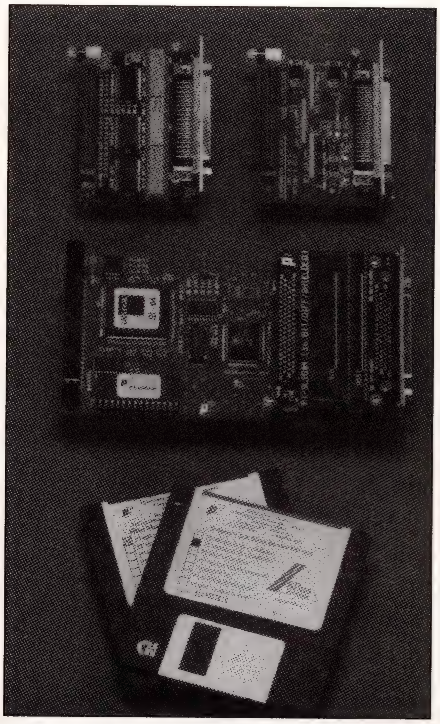
DSP and data acquisition come to Sbus. The SB-A220 provides two channels of 64×-oversampling delta-sigma A/D conversion with a dc to 22-kHz frequency range. It performs 25 Mflops using the 50-MHz AT&T DSP3210 processor. It comes with the SpectrumWare virtual-instrument software library and works with LabView for Sun workstations. The board costs $2495; LabView for Sun costs $3995. **National Instruments**, Austin. TX. (512) 794-0100.
Circle No. 504



VME board offers multiprocessor capability. Based on dual TMS320C40 DSP chips, the DSP220 6U VME board offers 80 Mflops of peak processing power. Each processor has 128 kbytes of EPROM and a 2k×16-bit dual-ported SRAM along with zero-wait-state program memory. The communications ports on the C40 connect to the VME P2 connector. $5495. **Olsson Research Inc**, Edmonds, WA. (206) 778-9480.
Circle No. 505

Board brings SCSI-2 to STD-32. The ZT 9855 offers the Fast-SCSI subset of SCSI-2 on an STD-32 card, handling 8- and 16-bit transfers to the bus. The device handles as many as seven SCSI peripherals and is software compatible with the Adaptec 1520/1520A. BIOS extensions and DOS-installable drivers are available. $375. **Ziatech**, San Luis Obispo, CA. (805) 541-0488.
Circle No. 506

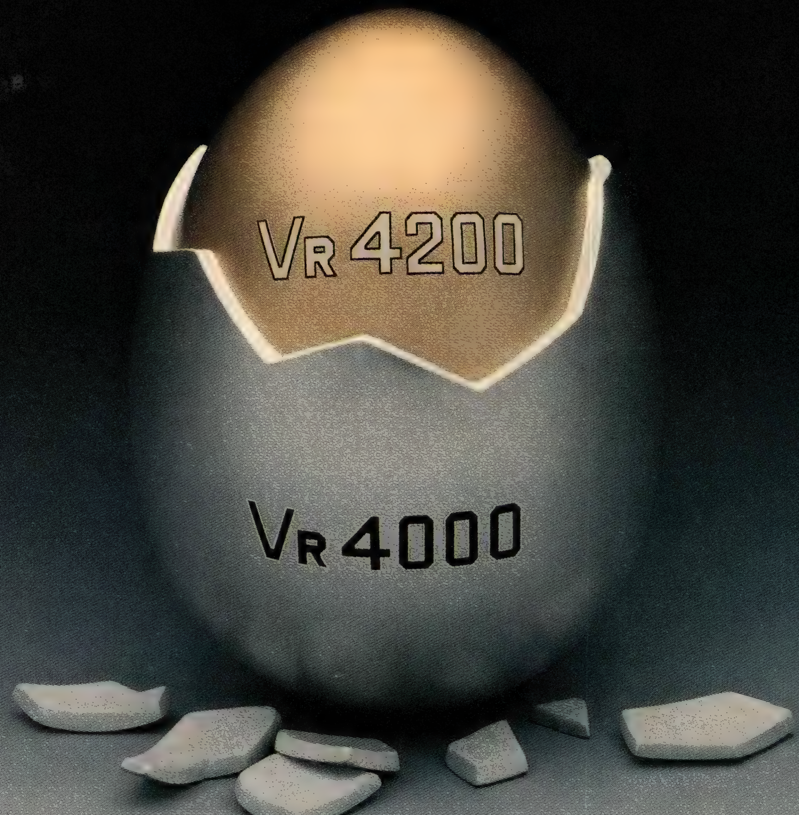
Mil-spec memory card holds 128 Mbytes. The SME-2, a 32-bit VME slave card for military applications, has four independent memory banks, each configurable for SRAM, EEPROM, or flash memory. It offers 5V standby operation and self-test capability. Prices start at $4775. **Radstone Technology**, Montvale, NJ. (201) 391-2700.
Circle No. 507



Adapter brings Wide/Fast SCSI-2 to Sbus. The PT-SBS440 adapter card provides 8- or 16-bit SCSI with single-ended or differential interfaces for Sun workstations. It handles as many as 15 devices and offers a 20-Mbyte/sec data-transfer rate. The board comes with Solaris 1.1 and 2.x software. From $995. **Performance Computer**, Rochester, NY. (716) 256-0200.
Circle No 508

Board tests 1553A/B-bus operation. The BusTools board plugs into an ISA-bus PC and allows testing of the MIL-STD-1553A/B data bus. It offers RT, BC, and concurrent monitoring of as many as four dual-redundant buses and can inject and detect errors at the word level. Monitoring capabilities include real-time recording of message and data contents, bus-loading statistics, and time tags. Including Windows-based setup and control software, $11,995. **Ponsor Corp**, San Diego, CA. (619) 597-0095.
Circle No. 509

Birth of a Winner



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The VR4200 is paced by an 80MHz internal clock. It delivers 55 SPECint92 and 30 SPECfp92. It incorporates a 16K-byte instruction cache and an 8K-byte data cache. Implemented with a 0.6µ triple-layer CMOS process and a smaller die, it runs on 3.3V and consumes only 1.5W. The VR4200 is available in a low-cost 208-pin plastic QFP or 179-pin ceramic PGA. It maintains hardware and software compatibility with the VR4000.

The VR4200 lets you build desktop capabilities into laptop and notebook computers. In combination with our RAB^{2}IT chip set (an I/O controller and memory controller for synchronous or Rambus DRAM), the VR4200 provides a cost-effective hardware platform for Windows NT.

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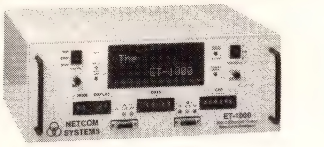

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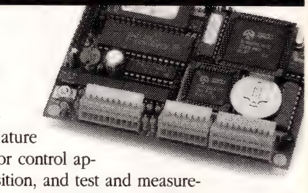

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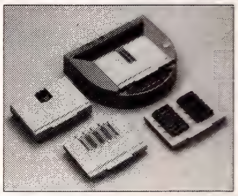

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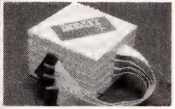

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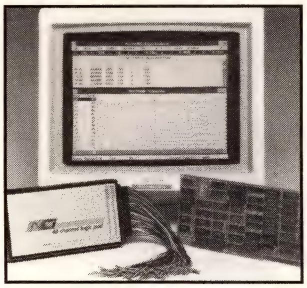

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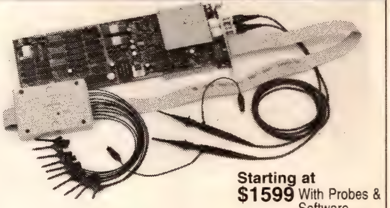

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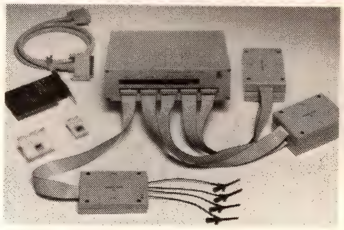

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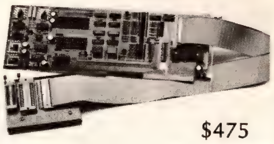

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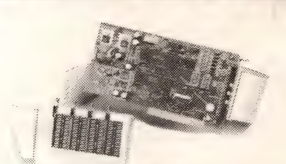

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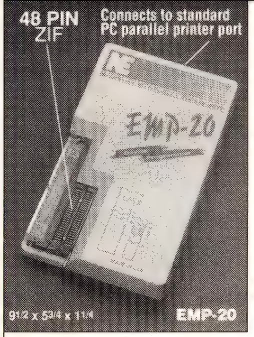

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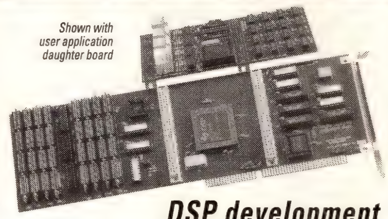
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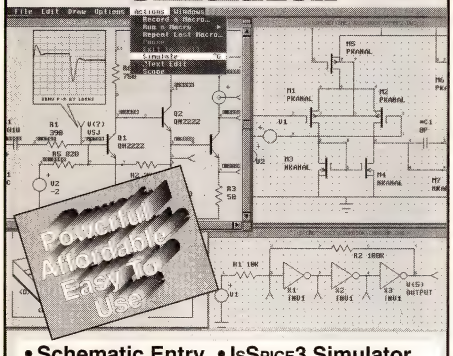

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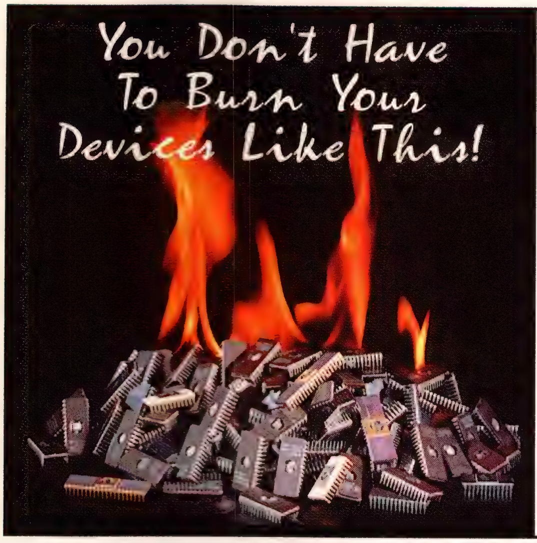

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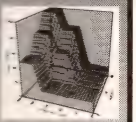

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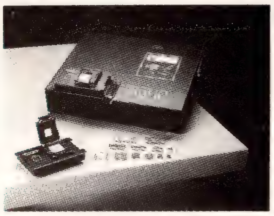

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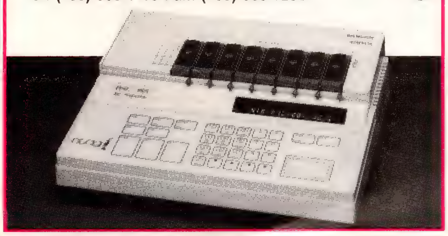

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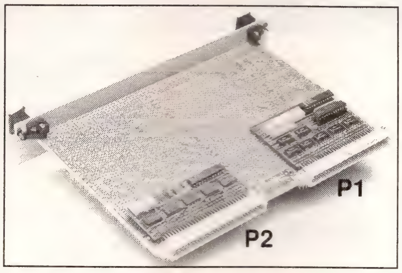

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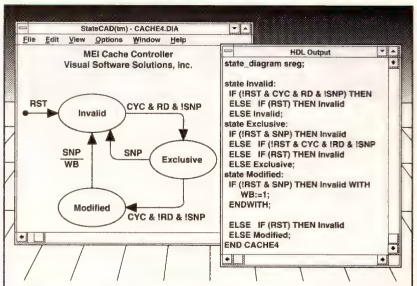

```
state_diagram sreg;

state Invalid:
  IF (!RST & CYC & RD & !SNP) THEN
   ELSE  IF (RST) THEN Invalid
   ELSE Invalid;
state Exclusive:
  IF (!RST & SNP) THEN Invalid
   ELSE  IF (!RST & CYC & !RD & !SNP
   ELSE  IF (RST) THEN Invalid
   ELSE Exclusive;
state Modified:
  IF (!RST & SNP) THEN Invalid WITH
      WB:=1;
   ENDWITH;

   ELSE  IF (RST) THEN Invalid
   ELSE Modified;
END CACHE4
```

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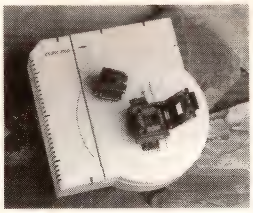

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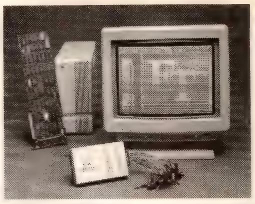

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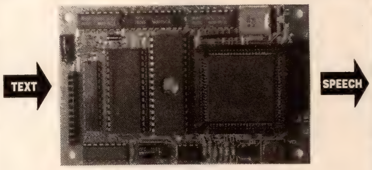

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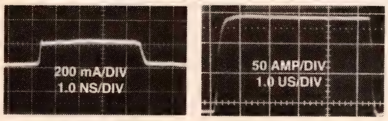

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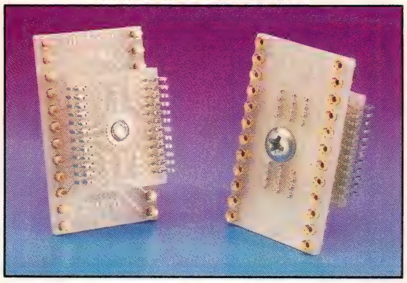

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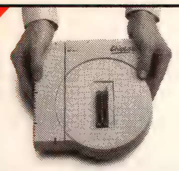

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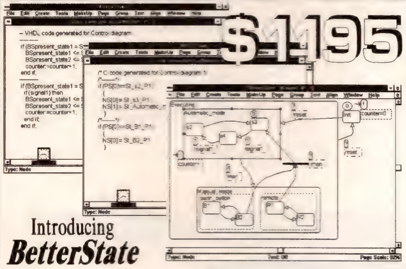

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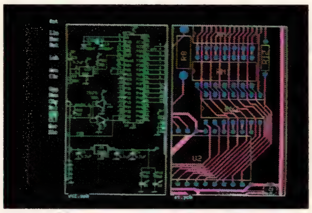

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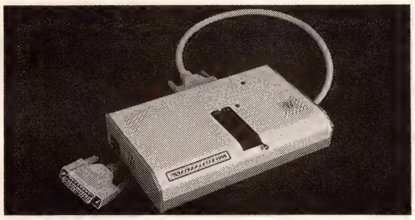

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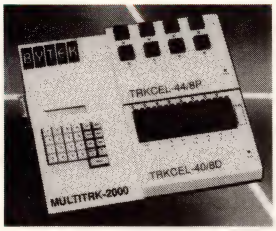

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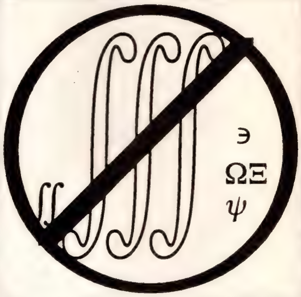

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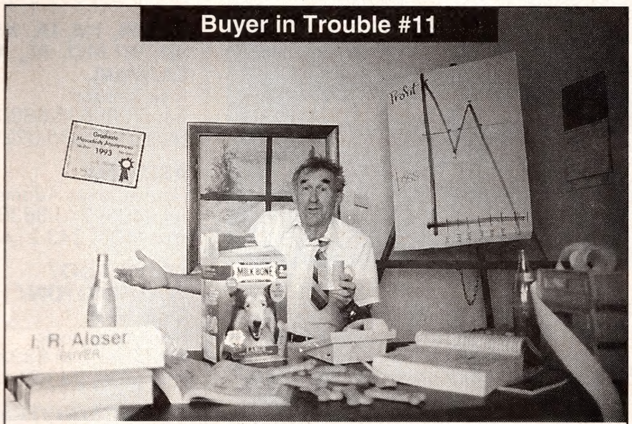

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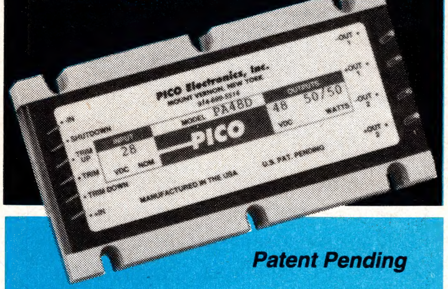

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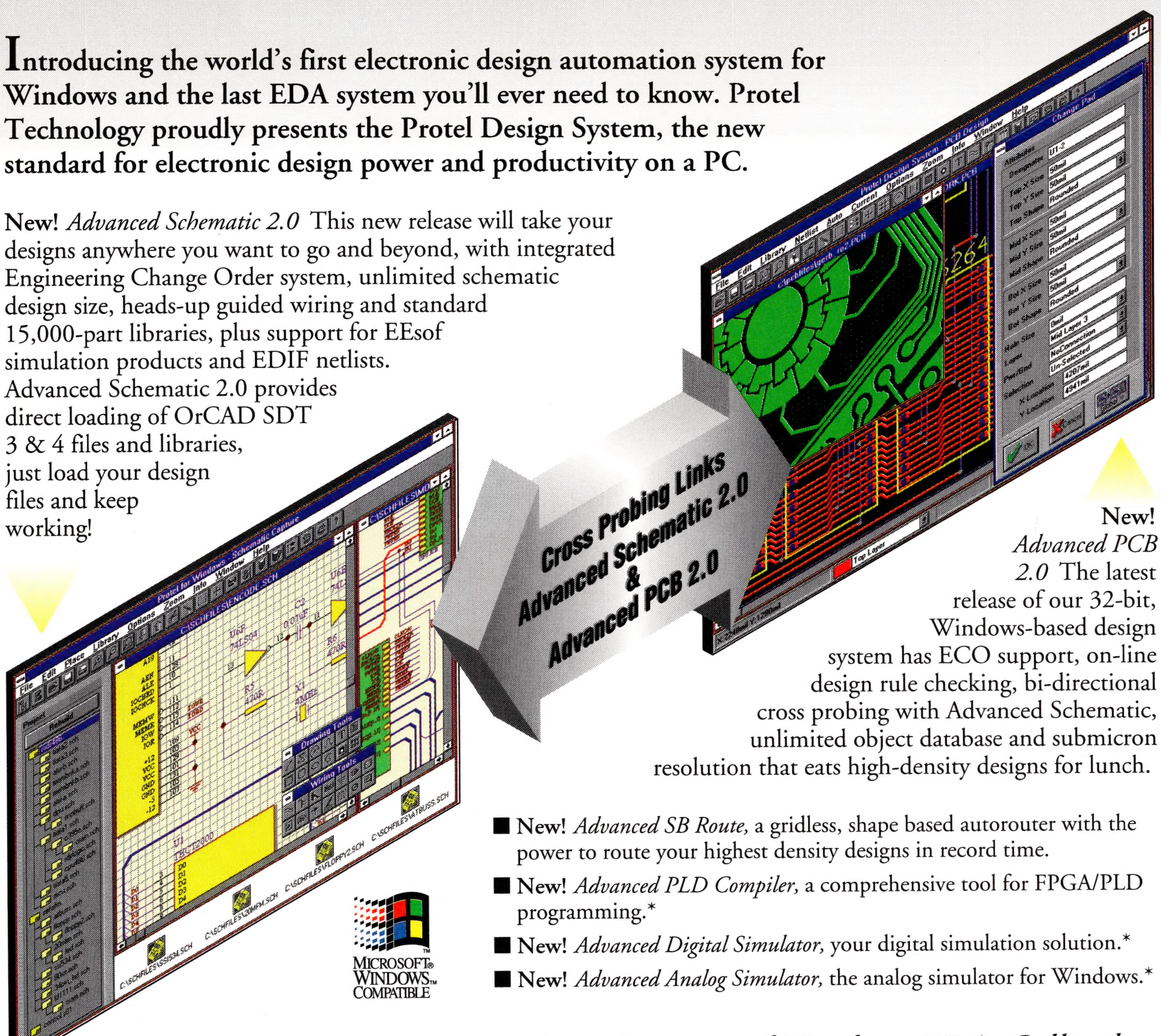
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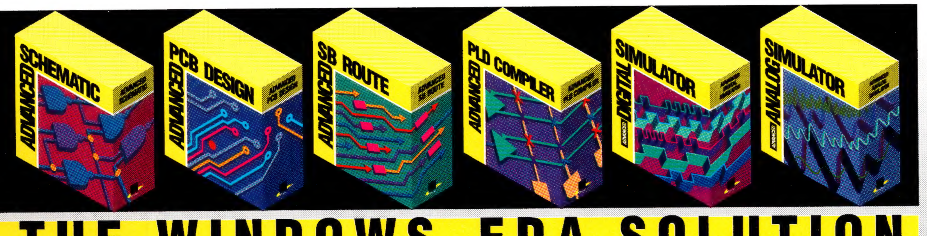

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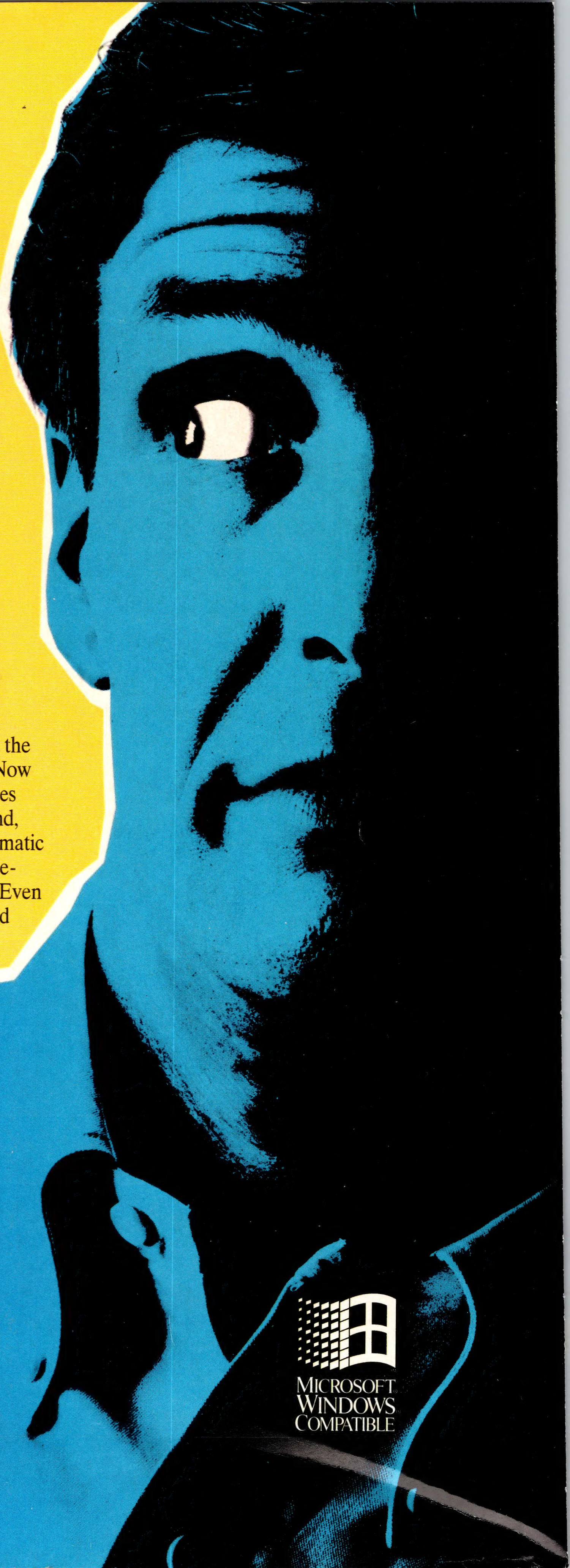

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